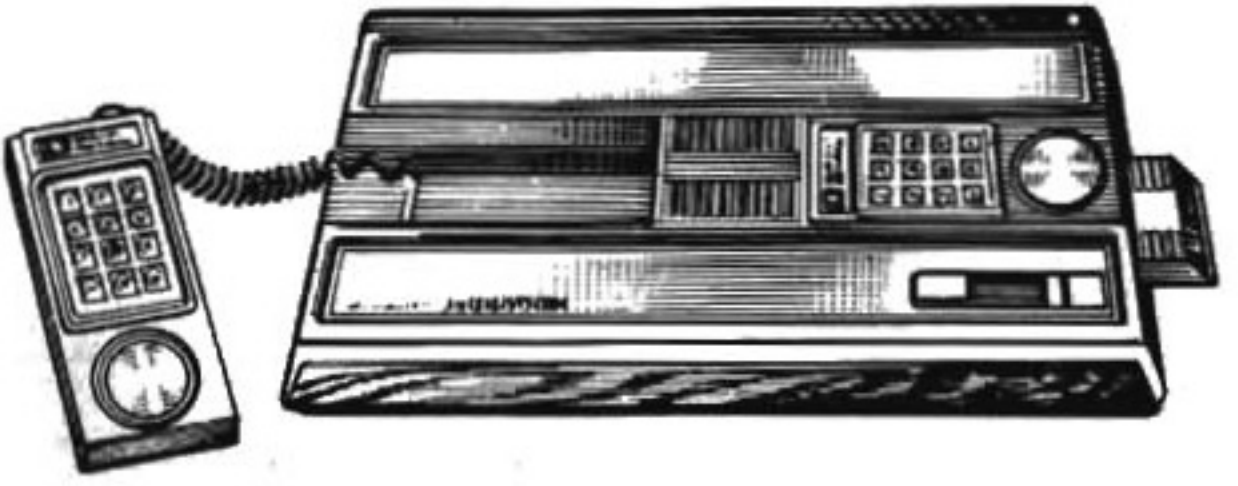
MATTEL ELECTRONICS®

SERVICE MANUAL



MODEL 2609

INTELLIVISION™

Intelligent Television

MATTEL ELECTRONICS
5150 Rosecrans Avenue
Hawthorne, California 90250

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SPECIFICATIONS

MICROPROCESSOR (CPU) — General Instrument CP-1610 16-bit processor

MEMORY — 7K internal ROM, RAM and I/O structures, remaining 64K address space available for external programs.

CONTROLS — Two hand controllers: 12-button numeric key pad, four action buttons, 16-position directional movement disc.

SOUND — Programmable sound generator (PSG) capable of producing three simultaneous sound patterns.

COLOR REPRODUCTION — 16 different color hues:

Black	Gray
Blue	Cyan
Red	Orange
Tan	Brown
Dark Green	Magenta
Light Green	Light Blue
Yellow	Yellow-Green
White	Purple

VIDEO RESOLUTION — 192 vertical X160 horizontal picture elements

PROGRAM MATERIAL — More than 24 different game cartridges available

VOLTAGE REQUIREMENTS — 120V AC 60 Hz.

DIMENSIONS (WxLxH) — 9" x 16¾" x 3"

WEIGHT — 7 lbs. with accessories in box

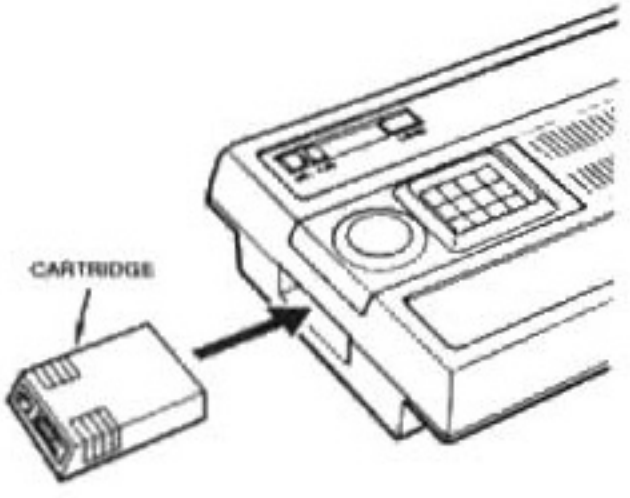
ACCESSORIES — Antenna Switch Box, Switch Box Cable (15 feet), 1 Game Cartridge with Instructions and 2 Mylar Controller Overlays

OPERATING INSTRUCTIONS

(A) Connection to color television receiver:

1. Connect the twin lead from the antenna switch box to the VHF antenna input of the television receiver.
2. Connect the RF cable from the RF output jack on the master component to the game input jack on the antenna switch box. Place the switch on the switch box to the game position.
3. Set the television receiver to CH 3 or 4, whichever is not used in your broadcast area. Place the RF channel select switch (located on the bottom of the master component) to the proper channel to correspond to the channel set on the television.
4. Plug the AC power cord into a 120V AC 60Hz source.

(B) 1. Insert the game cartridge in the slot located on the right side of the Master Component. Refer to the diagram below:



2. Remove the Hand Controllers from their holder on the Master Component.
3. Slide the ON-OFF Switch to the ON position and depress the RESET switch located on the Master Component.

Hand Controller

(C) The Hand Controllers

The Master Component contains two Hand Controllers which are permanently attached with coil cables. You will notice that there are 12 keys on the keypad. These are used for feeding data into the Master Component.

With each cartridge, there are 2 overlays which fit over the keypads of the 2 Hand Controllers. These overlays are keyed to the particular game being played and determine how the keys on the keypad relate to the cartridge. Slip the overlay under the keypad frame as shown. Some Hand Controllers have a lip at the top of the controller which will prevent the overlay from being pushed back out during normal game play.

There are 2 action buttons on each side of the Hand Controller. The top buttons, 1 on each side, perform the same function for the convenience of either right or left handed players. The bottom buttons perform varying functions. The functions of all the buttons depend on the cartridge being used and are different for each cartridge overlay.

The disc at the base of the Hand Controller is a directional control for those cartridges in which direction is a factor. There are 16 directional positions on the disc. Direction of disc corresponds to direction on television screen. UP on the disc (toward the keypad) is UP on the screen, etc. For further instructions refer to your cartridge instructions.

To operate the directional disc, press your finger on the outer edge and slide your finger around the edge to change direction of object you are moving. You have the ability to move the object in any direction you wish. To stop motion, simply stop pressing the disc. You must be pressing on the disc in some direction for motion to take place.

The keypad buttons and directional disc cannot be operated simultaneously. However, the action buttons and directional disc can be. See cartridge instructions.

When returning the Hand Controller to the Master Component, coil the cable beneath it in the cradle.

To avoid permanently overstretching the coiled cables, they should not be pulled out to their extreme length.

(D) THE INTERMISSION CODE AND THE AUTOMATIC BLANK SCREEN

If for any reason you wish to interrupt your game, you may use the Intermission Code (remove game overlay and depress 1 and 9 keypads simultaneously on either Hand Controller). The television screen will then go blank. To resume game play, simply depress any key on either Hand Controller. Also, the Master Component will automatically blank the television screen if no functions on the Hand Controller are activated after approximately 5 minutes. Again, to resume game play, simply depress any key on either Hand Controller. The purpose of this unique feature is to eliminate the possibility of a permanent playfield image being imprinted on your television screen.

NOTICE TO PROJECTION TV OWNERS: Operating the Master Component for extended periods of time on a projection TV system may cause the stationary game objects to become permanently imprinted on the projection TV picture tube(s). This is especially true when brightness and contrast controls are set extremely high for game viewing. Observing the following procedures will greatly minimize the chances of a game image being retained on the screen:

1. Always use lowest possible brightness and contrast control settings during game operation.
2. Games containing stationary white or light colored objects should not be played for extended periods of time.
3. Follow your projection TV owner's manual for proper viewing conditions for programming.

SECTION I
SYSTEM DESCRIPTION AND OPERATION

1-1. GENERAL. The Master Component (See Figure 1-1) is the fundamental component in the Mattel Intellivision system. It consists of a console assembly with two hand controllers, an antenna switch box, and a switch box cable. The Master Component is designed to operate in conjunction with a color television set and an Intellivision game cartridge.

1-2. The Master Component system is based on two processors. One is a 16 bit microprocessor (CPU) that computes the game action against the stored program rules. The second is the Standard Television Interface Circuit (STIC) that interprets a condensed memory area and uses this to generate a color video signal. The video signal is applied to the RF modulator to provide a television signal. The user's color television receiver is used for the video display.

User interaction with the game programming is accomplished by the inputting of numerical control and directional information through the hand controllers.

The audio is accomplished by using a programmable sound generator (PSG) IC that generates the audio signal to drive the RF modulator. The user's television receiver is used for the audio output.

1-3. CONSOLE ASSEMBLY. The Console Assembly contains all electrical circuitry necessary for recall and processing of program data stored in the game cartridge. Integral with the console assembly are the power transformer and ON/OFF switch assembly, power supply board assembly, logic board assembly and two hand controller assemblies. Recessed compartments in the top of the console are provided for storage of the hand controllers and cables. A slot in the right-hand side of the console assembly is the insertion point for the game cartridge. The power ON/OFF switch and a reset button are located in the lower right-hand corner of the console assembly.

a. Power Transformer and On/Off Switch Assembly. The power transformer and on/off switch assembly consists of a power transformer with an internal primary fuse, two secondary windings, a triple-pole single-throw switch and associated wiring. Electrical connection to the power supply board assembly (PCB Power Supply) is accomplished via a 5-pin electrical connector which provides the AC voltages for operating the power supply board assembly.

b. Power Supply Board Assembly. The power supply board assembly (PCB Power Supply) consists of two regulator/heat sink assemblies and the necessary related components mounted on a printed circuit board. Electrical connection to the logic board assembly is accomplished via a 5-pin electrical connector and a 2-pin electrical connector. The power supply board rectifies the AC voltages from the power transformer and supplies regulated and nonregulated DC voltages to the logic board assembly (PCB LOGIC).

c. Logic Board Assembly. The logic board assembly (PCB LOGIC) consists essentially of 17 integrated circuits and necessary related components, a crystal oscillator clock timer and associated variable capacitor, a channel select switch and an RF modulator, all of which are mounted on a printed circuit board. A 44-pin connector is provided for game cartridge connection. Two 9-pin connectors are provided for connection of the hand controllers. The PCB LOGIC is enclosed by a two-piece metal shield that provides RF shielding. The logic board processes program data from the game cartridge and converts the processed data to an RF signal for color television operation.

d. Hand Controller Assemblies. The hand controller assemblies each consist of a printed circuit matrix, a domed legend (numerical key pad), two side-mounted double push-buttons and a 16-position directional control disc. The hand controllers provide a means of calling up program information from the game cartridge for processing by the CPU.

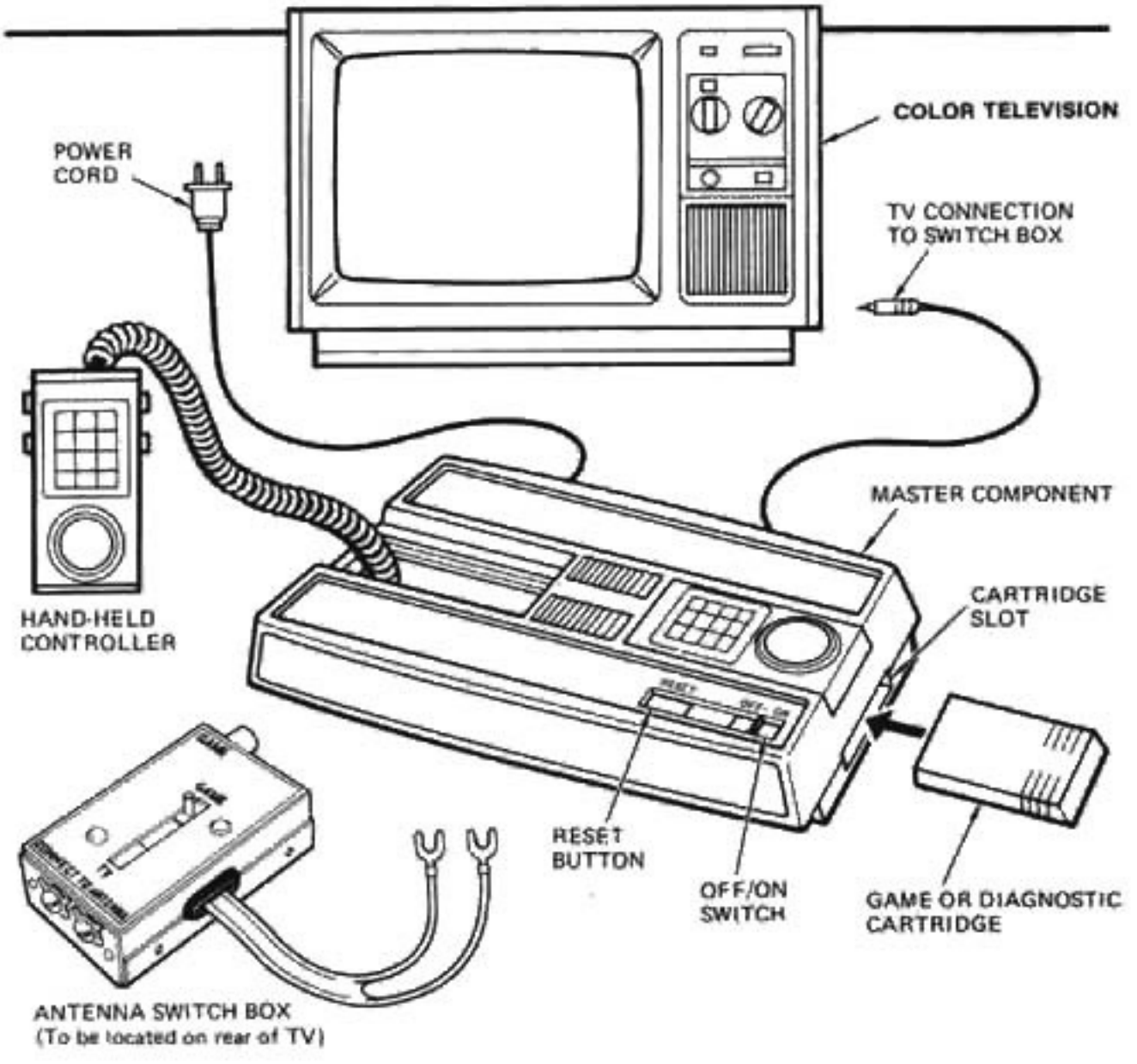


Figure 1-1. Mattel Intellivision Master Component

1-4. ANTENNA SWITCH BOX AND CABLE. The antenna switch box provides the interface between the console assembly and television set. The switch box cable is connected between the console assembly and switch box. Two spade lugs on the switch box are provided for connection to the television set. Two screws on the switch box are provided for connection to the television antenna. The antenna switch box serves to select either the console assembly or the external antenna as the source of RF input to the television antenna input. For 75Ω antenna systems a balum transformer is required.

1-5. THEORY OF OPERATION. The following paragraphs provide functional theory of operation for the Master Component. Detailed operational characteristics for PCB LOGIC IC's, RF modulator and the power transformer are provided in Section 7. Schematic diagrams for the PCB Power Supply and PCB LOGIC are also provided in Section 7. Figure 1-2 is a functional block diagram of the Master Component.

1-6. The system is based on the use of two processors which time-share a 14-bit bidirectional bus. The central processing unit (CPU), Type No. CP1610, algorithmically computes the game action against program material stored in the ROM game cartridge. The standard television interface chip (STIC), Manufacturer's Type No. AY-3-8900-1, interprets a condensed memory area and uses the information to generate the television raster display. The STIC also fetches moving and background picture information from the graphics memory and presents the data as a video output. The video output is applied to an RF modulator for color television display.

1-7. CENTRAL PROCESSING UNIT (CPU). The CPU is a complete, 16-bit, single chip, high-speed metal oxide semiconductor, large scale integrated circuit (MOS-LSI) microprocessor. It utilizes a 16-bit bidirectional bus to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices. Timing and synchronization signals are applied to the CPU by the STIC. CPU bus control outputs serve to define the status of bus operations.

1-8. STANDARD TELEVISION INTERFACE CHIP (STIC). The STIC, Manufacturer's Type No. AY-3-8900-1, operates within the system by time-sharing a 14-bit bidirectional bus. The main STIC function provides eight coordinate-positioned "foreground" objects. The second function provides a background display facility. The "background" mode utilizes a dedicated area of external memory to store character control codes for each display position. Both modes utilize external memory for the storage of character patterns. The STIC accepts data, address and graphics information from a common multiplexed bus. Demultiplexing and system synchronization are accomplished through three sets of control signals.

1-9. The main synchronization (which operates at television frame rate) synchronizes the CPU algorithms to the intended display sequences, obtains "background" character descriptors from the external memory and serves to enable external devices onto the 14-bit bus when in the CPU-controlled mode. The second set of control signals is used to specify address, read and write for external memory where graphic character patterns are stored. When in the CPU-controlled mode, the graphics control bus links the graphics memory to the CPU main memory. The third set of controls is used to specify address, read and write sequences to the STIC when the system is in the CPU-controlled mode. Video output codes from the STIC are applied to the color oscillator/master clock generator for processing.

1-10. GRAPHICS MEMORY. The graphics memory consists of a graphics read only memory (ROM), Manufacturer's Type No. RO-3-9503, and two graphics random access memories (RAMs), Manufacturer's Type No. 3539. The two graphics RAMs are connected to the graphics ROM by an 8-bit static address bus. Address, read and write sequences are applied to the graphics ROM by the STIC. Output from the graphics memory is applied to the 14-bit secondary data bus.

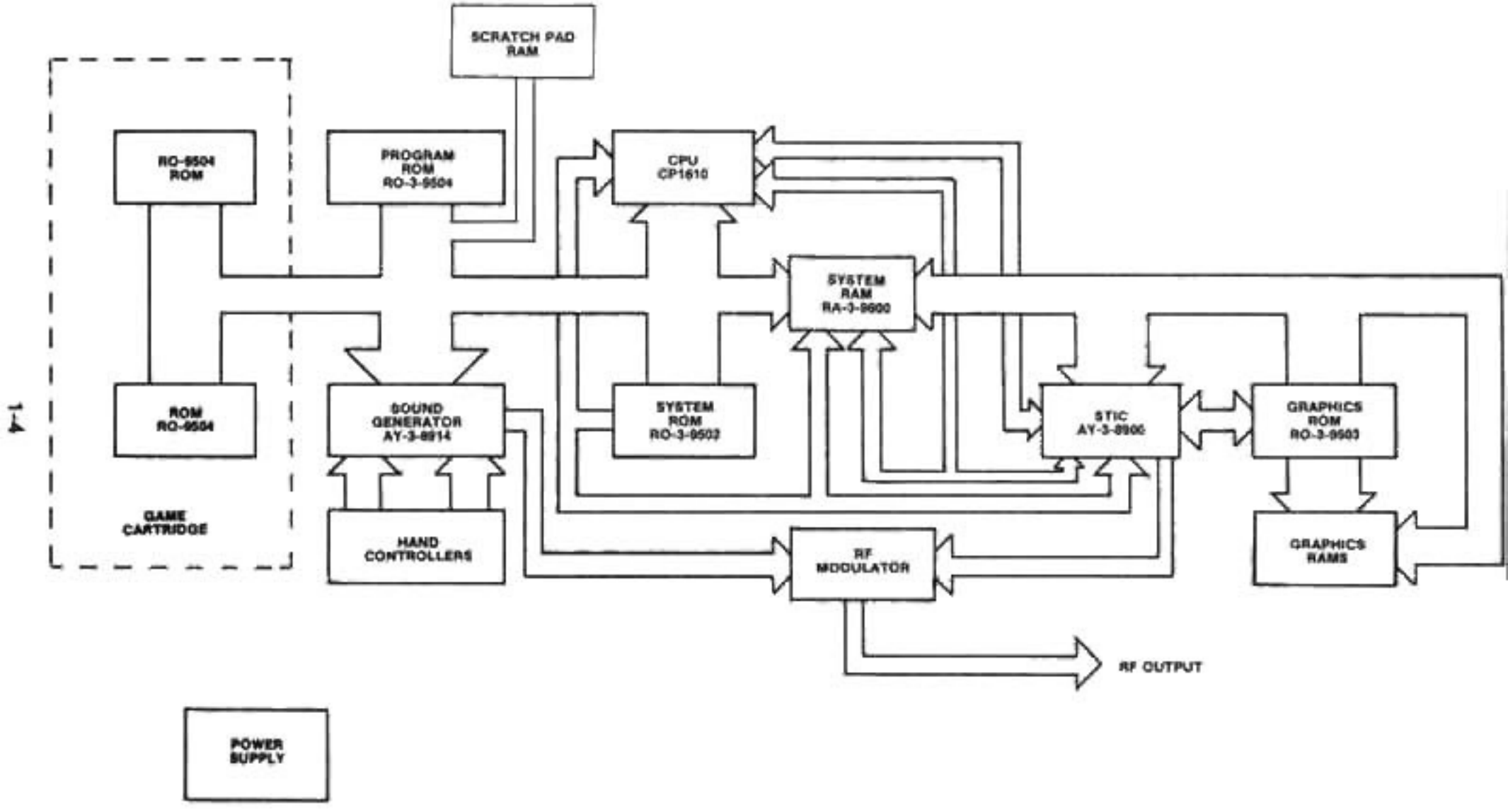


Figure 1-2 System Block Diagram

1-11. COLOR OSCILLATOR/MASTER CLOCK GENERATOR. The color oscillator/master clock generator, Manufacturer's Type No. AY-3-8915, decodes video inputs from the STIC and generates clock signal for system control. Oscillator frequency input is applied by a 7.159090 MHz crystal with an associated trimmer capacitor. The clock generator provides a 3.579545 MHz clock signal output. Video information from the STIC is applied to five inputs to produce composite sync, color burst, line blanking, screen blanking and video outputs. The analog outputs of the color oscillator are combined by four external precision resistors to provide a composite video signal to the RF Modulator.

1-12. SYSTEM RANDOM ACCESS MEMORY (SYSTEM RAM). The System RAM is a dual port interface, 16-bit wide storage area which serves as the control decoder for CPU control data. The System RAM receives data from the CPU via a 16-bit bidirectional time-multiplexed bus. The direction of data travel is always from the CPU to the graphics memory except during a bus reversal condition. This condition is indicated when the CPU requests a read from a graphics address on the 14-bit graphics bus. A 3-bit control bus from the CPU provides strobe signals to the System RAM for the on-chip address latch and main memory area.

1-13. PROGRAM READ ONLY MEMORY (PROGRAM ROM). The internal program area is comprised of an executive ROM, Manufacturer's Type No. RO-3-9502, and a scratch pad memory, Manufacturer's Type No. 3539, associated with the program ROM. The executive ROM contains system operating data. System program data from the executive ROM is transmitted along a 16-bit bidirectional data bus. The program ROM contains program data common to all external programs. Data from the program ROM is transmitted along a 16-bit bidirectional bus. A scratch pad memory RAM associated with the program ROM is provided for computation of Program ROM data. Interconnection of the program ROM and the scratch pad memory RAM is accomplished through a 14-bit bidirectional data bus.

1-14. PROGRAMMABLE SOUND GENERATOR. The programmable sound generator (PSG), Manufacturer's Type No. AY-3-8914, is a large scale integrated circuit (LSI) designed to produce a wide variety of sounds. All control signals to the PSG are provided by the CPU. Two 8-bit general purpose I/O ports are provided for user interface via the hand controllers. PSG output is applied at three independently programmed analog outputs. The output of the PSG is applied to an RF modulator for audio output through a television set.

SECTION 2
SYSTEM TESTING AND TROUBLESHOOTING

2-1. DIAGNOSTIC TEST ROUTINE. The diagnostic routine should be performed before disassembly of the Master Component. Perform the diagnostic test routine as described below:

a. Test Procedure. Upon insertion of the MTE-201 Test Cartridge and depressing the reset button on the Master Component (M/C), the unit will proceed through a series of checks on the CPU (UI) and areas accessible by it. This automatic test sequence takes approximately 10 seconds to complete.

(1) At the completion of the above test sequence, the Hand Controller test display will appear as shown in Figure 2-1.

(a.) Press each key on the Hand Controllers, one at a time and verify that each corresponding test image turns from yellow to white when the appropriate key is depressed. NOTE: The right Hand Controller will affect the left test image and vice versa.

(b.) Press the top side buttons on the Hand Controllers one at a time. Make sure that the pair of Fs change from yellow to white.

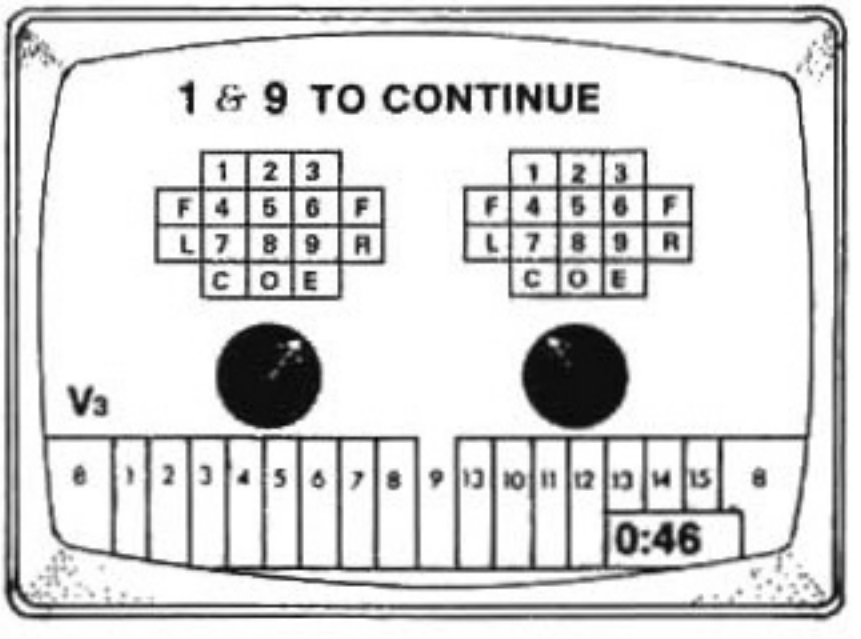
(c.) Press each lower side button on the Hand Controllers one at a time and see that the letters L and R change from yellow to white.

(d.) Depress the directional disc on each Hand Controller and a white arrow will appear in the black circle. As the directional disc is rotated, the arrow will rotate. Check to see that the arrow points in 16 different directions.

(e.) Check the row of colored boxes for similarity as listed in Figure 2-1.

If any of the operations do not occur as described it indicates either a defective Hand Controller or Sound IC (U6).

Next, depress the digit keys 1 and 9 simultaneously on either Hand Controller and the test sequence will proceed to the sound checks.



COLOR CODE:
1. Black
2. Blue
3. Red
4. Tan
5. Dark Green
6. Light Green
7. Yellow
8. White
9. Gray
10. Orange
11. Brown
12. Magenta
13. Light Blue
14. Yellow/Green
15. Purple

Figure 2-1 Hand Controller Test Pattern

(2) Verify that the following sequence of sounds is heard:

(a.) A high note stepping down through five octaves (repeated three times).

(b.) Random noise (hissing) starting at a high volume and diminishing until silenced.

(c.) A single tone, starting at a high volume and diminishing slowly.

(d.) Two gunshots, one at normal volume, the second at half volume.

If all of these sounds are heard as described, depress the CLEAR key on either Hand Controller. In the event any part of the test has failed, depress the ENTER key. (NOTE: The test sequence cannot be advanced if the CLEAR or ENTER key is depressed while sounds are being generated.)

(3) The next segment of the test presents a series of patterns, ending with the pattern illustrated in Figure 2-2. Check colors in the test pattern against Figure 2-2 for similarity and definition. If test pattern accuracy is satisfactory, press the CLEAR key. If it is unsatisfactory, press the ENTER key.

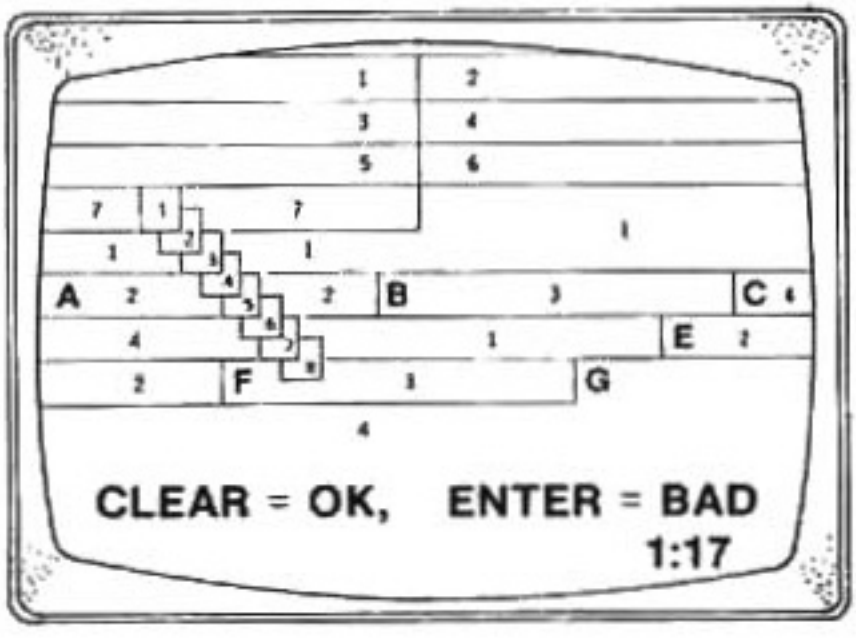
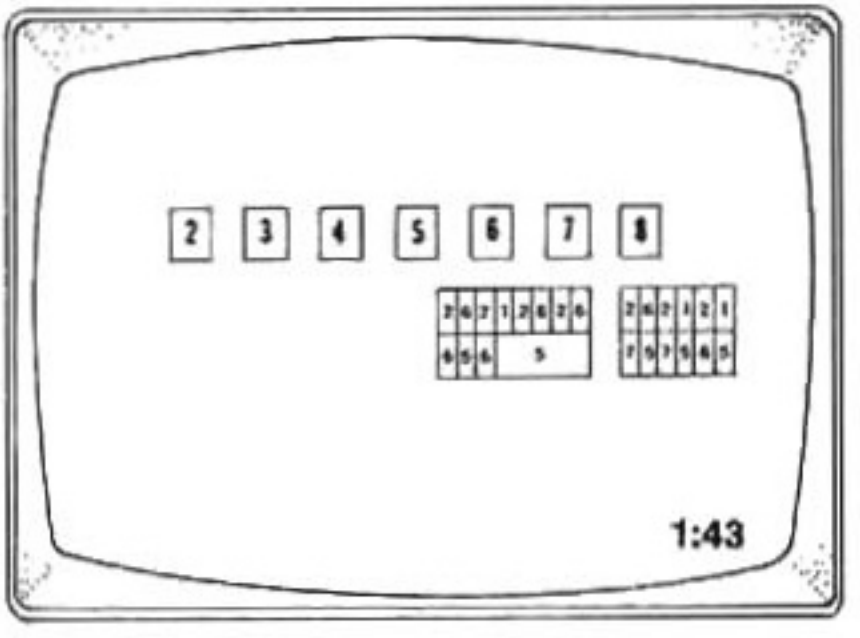


Figure 2-2

(4) The next portion of the test sequence is a pattern of colored blocks with the two larger blocks alternating with the words MODE TWO on a red background, as illustrated in Figure 2-3. Check colors in test pattern against Figure 2-3 for similarity and definition. If test pattern accuracy is satisfactory, press the CLEAR key. If it is unsatisfactory, press the ENTER key.



COLOR CODE:
1. Black
2. Blue
3. Red
4. Tan
5. Dark Green
6. Light Green
7. Yellow
8. White
9. Gray
10. Orange
11. Brown
12. Magenta
13. Light Blue
14. Yellow/Green
15. Purple

Figure 2-3

(5) The last pattern of the test alternates between the letters F/B and VIS. Press the CLEAR key for a satisfactory indication. Press the ENTER key for an unsatisfactory condition.

If no failure has been detected, the title page for Baseball will appear; this indicates the M/C has passed all the automatic and operator tests.

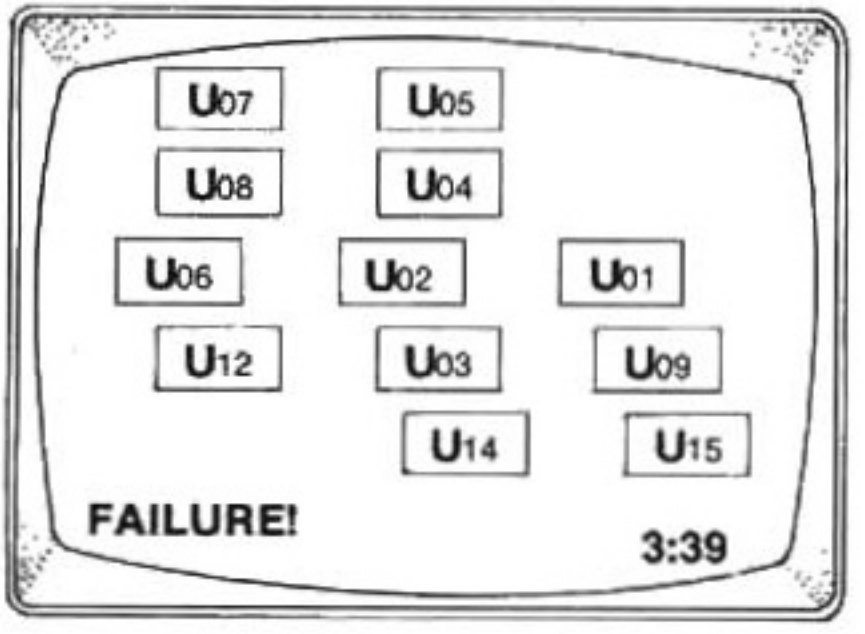


Figure 2-4

In the event a failure has been detected, instead of the title page being displayed, a display as shown in Figure 2-4 will appear. Depending on the failure code detected, the suspect IC will flash in Red and Blue indicating the most likely defective IC.

The next test is an actual game check to confirm the functional operation of the M/C. When the title page for Baseball is displayed, follow the instructions provided with the MTE-201 Test Cartridge to play ½ an inning of baseball.

Upon successful operation of the baseball game, the test routine for the Master Component is complete.

The reason the Baseball game is utilized is because the Baseball makes full use of the digital/memory facilities of the M/C.

MTE-201 FAILURE CODES AND CAUSES

FAILURE CODE	DESIGNATED IC	DESCRIPTION	OTHER POSSIBLE IC FAILURES
A	U5 (GROM)	Check SUM Graphics ROM	U2, U4, U9
B	U9 (SROM)	Check SUM System ROM	U1
C	U3 (PROM)	Check SUM PROGRAM ROM	U1
D	U4 (STIC)	Memory test of STIC	U2, U5
E	U8 (LGRAM)	Memory test of Lower Graphics RAM	U4, U5, U2
F	U7 (UGRAM)	Memory test of Upper Graphics RAM	U4, U2, U5
G	U2 (SRAM)	Memory test of SYSTEM RAM	U4, U5, U1
H	U12 (SPAD)	Memory test of SCRATCHPAD RAM	U9, U1, U3
J	U6 (PSG)	Memory test of Sound IC	U9, U1, U3
K	U4 (STIC)	Interaction test of STIC IC	
N	U4 (STIC)	"Solid Test" verifies that all 64 points on all 8 moving objects react to interaction	U2
O	U4 (STIC)	Verifies that all 4 quadrants of the colored squared mode register interactions in all colors, but clear.	U1
P	U4 (STIC)	Verifies that the top left and bottom right corner of the screen register proper interaction at all offset positions.	
Q	U4 (STIC)	Uses interactions to verify that X zoom functions.	
R	U4 (STIC)	Uses interactions to verify that Y zoom functions.	
S	U4 (STIC)	Uses interactions to verify that Y mirror functions.	
T	U4 (STIC)	Uses interactions to verify that X mirror functions.	
U	U4 (STIC)	Uses interactions to verify that full/half height objects functions.	
V	U4 (STIC)	Uses interactions to verify that 8/16 line objections functions	U2
*W	U4 (STIC)	Color priority test	
*X	U6 (PSG)	Manual fail of audible test	
*Y	U4 (STIC)	Manual fail of visibility of foreground/background priority	
*Z	U4 (STIC)	Manual fail of mode one/mode two visual	

*Pass or failure is determined by operator/technician performing test.

NOTE: IF MULTIPLE FAILURE OCCURS, SEE THE RECOMMENDED SUBSTITUTION SEQUENCE FOR LOCATING THE DEFECTIVE ICs (Pg. 2-9)

When the Hand Controller test is displayed, instead of depressing keys 1 and 9 simultaneously to continue the test sequence, you may access the following programs:

INDIVIDUAL TESTS:

Depress keys 1 and 7 simultaneously and an individual test menu is displayed. The left Hand Controller is then used to enter the selection number to determine the test to perform.

Depress the CLEAR key to remove erroneous selection number entry.

Depress the ENTER key after the input of the selection number, to perform the entry selected

The tests are as follows:

Selection No.	Test Performed
0.	Return to Hand Controller test display.
1.	STIC Automatic Tests—Perform the tests on the STIC which do not require operator intervention. These tests are those of which valid responses from the STIC itself can be detected by the CPU.
2.	Memory test of the System RAM.
3.	Memory test of the Sound IC (PSG).
4	Check SUM test SYSTEM ROM (SROM).
5	Check SUM test PROGRAM ROM (PROM).
6.	Check SUM of GRAPHICS ROM.
7.	Memory test of the LOWER GRAPHICS RAM.
8.	Memory test of the UPPER GRAPHICS RAM.
9.	Memory test of the SCRATCHPAD RAM (SPAD).
10.	Audible test of Sound IC (PSG).
11.	Visual verification test.

Upon successful completion of some of the individual tests selected, a small Blue symbol will appear at the bottom of the display. If a failure is detected, a failure code will be displayed on the screen. To exit the program, select 0, which will return the operator to the normal test routine.

TEST CARTRIDGE CHECK:

Depress keys 2 and 8 simultaneously and a checksum for the MTE-201 test cartridge will be displayed. The display should look like this.

"CART CHECKSUM LO = "
"00002371677"
"CART CHECKSUM HI = "
"00003372642"

If any other numbers appear or the numbers differ, it indicates a failure in the test cartridge and another cartridge should be utilized.

2-2. CUSTOMER'S GAME CARTRIDGE TEST. Test the customer's Game Cartridge as follows:

a. Verify that Master Component is connected to television set as outlined in the operating instructions (Page 01-1).

b. Set the Antenna Switch Box to GAME. Insert customer's Game Cartridge in Master Component and depress the reset switch. Check for mistake in lettering on title picture, jumbled playfield or unwanted characters.

c. If problems occur, remove customer's Game Cartridge and check Master Component with a known-good Game Cartridge.

d. With the known-good Game Cartridge inserted, if problems are not observed, then the customer's Game Cartridge is defective. If problems are still observed, troubleshoot the Master Component.

2-3. RECOMMENDED TEST EQUIPMENT

1) Dual Trace Oscilloscope
2) Digital Multimeter
3) Frequency Counter
4) Color Television
5) Heat Gun
6) Diagnostic Test Cartridge (MTE-201)
7) Basic Electronic Hand Tools including Soldering/Desoldering Equipment

2-4. POWER SUPPLY TEST. Test the PCB-Power Supply as follows:

a. Disassemble the Master Component in accordance with Section 3-3, steps a. through f.

b. Plug in Master Component (M/C) power cord and set Power ON/OFF switch to ON

c. Refer to Figure 2-5 PCB-Power Supply test points locations. With a DVM check for +5V ± 0.15V DC at TP2. (The voltages are referenced to ground TP1.)

d. Check for +12V DC ±0.36V DC at TP3.

e. Check for +18V DC ± 1.25 DC UNLOADED at TP4 (nonregulated +16V DC source).

f. Check for -2.1V DC ± 0.15V at TP5 (early production units below serial number 113899, the voltage will be -3.3V DC. CR9 is a 3.3V zener diode in early production units).

g. If all the voltages are correct as specified above, troubleshoot the PCB-LOGIC assembly. If any incorrect voltage measurements were obtained above, proceed with the following steps to isolate the defect:

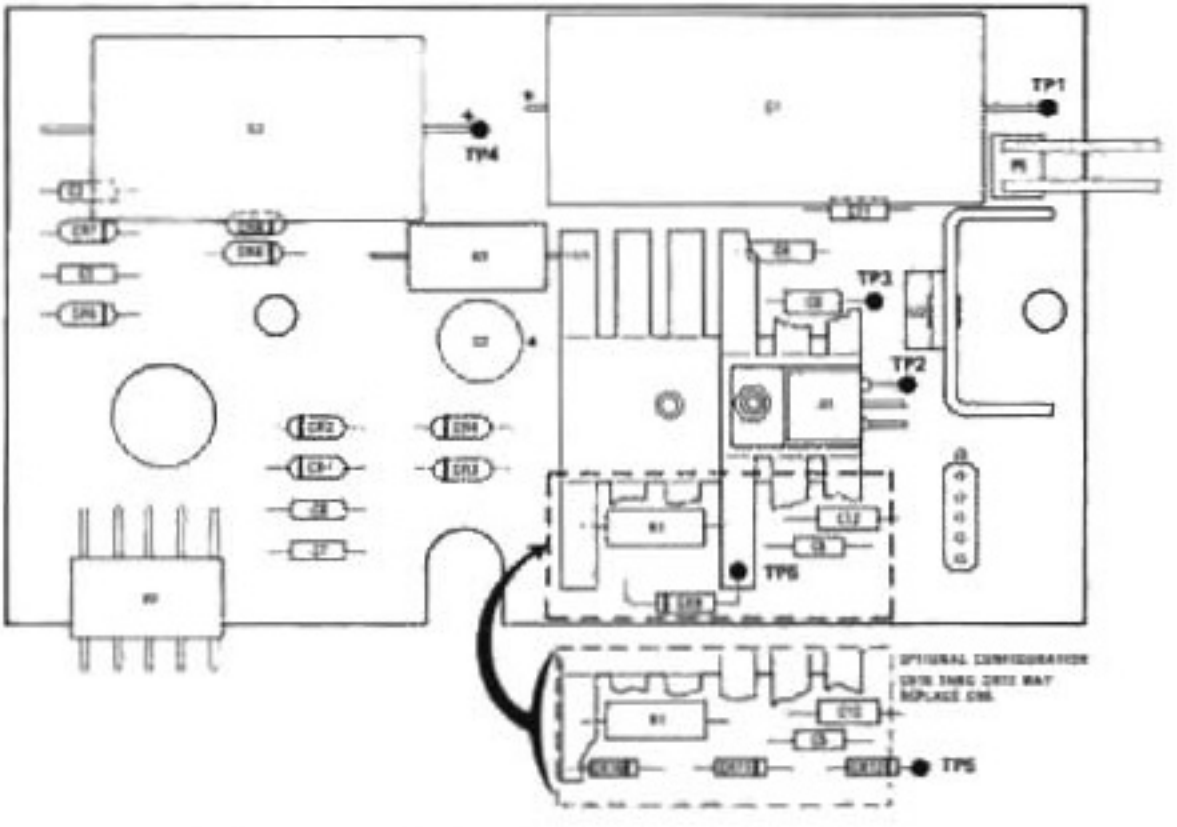


Figure 2-5 Test Points Location Diagram

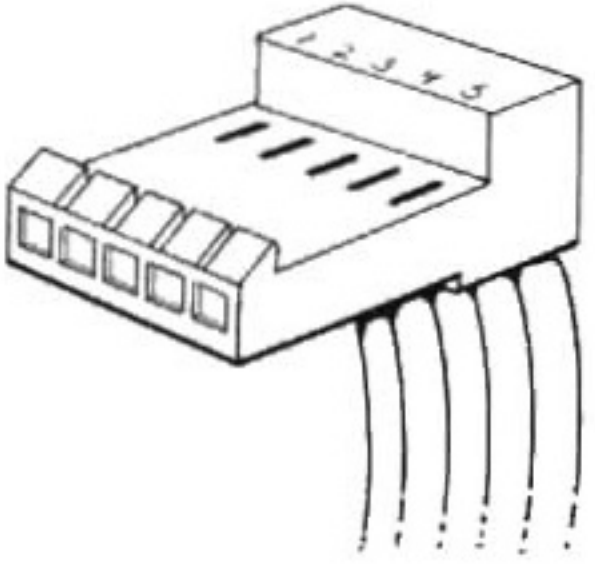
TP-1 ..... GROUND
TP-2 ..... +5V DC TEST
TP-3 ..... +12V DC TEST
TP-4 ..... +16V DC TEST (Non-Regulated)
TP-5 ..... -2.1V DC TEST (Early Production -3.3V)

h. Disconnect the 5-pin connector (17, Figure 6-1) of the power transformer assembly from the PCB-Power Supply. With a DMM measure the AC voltage across pins 1 and 3 of the connector. The AC voltage should be between 7.6 and 9.4V AC RMS.

i. Verify that the AC voltage across pins 2 and 3 of the connector is between 7.6 and 9.4V AC RMS.

j. Verify that the AC voltage across pins 4 and 5 of the connector is between 15.3 and 18.7V AC RMS.

k. If the AC voltage measurements are within the specified limits, troubleshoot the PCB-Power Supply. If the AC voltages are not correct, check or replace the power transformer, ON/OFF switch, wiring assembly.



NOTE: IF THIS PLUG DIFFERS FROM THE TYPE ENCOUNTERED, REFER TO WIRING DIAGRAM IN SECTION 5 FOR CORRECT PIN IDENTIFICATION.

2.5 MATTEL INTELLIVISION MASTER COMPONENT TROUBLESHOOTING GUIDE.

This guide is provided as an aid for troubleshooting the MATTEL INTELLIVISION MASTER COMPONENT. The guide contains a chart listing the problems usually affecting the Master Component, the causes of the problems and guidelines for correcting the problems. This guide has been written with the assumption that the servicing technician has the ability to follow good electronics troubleshooting practices and procedures, especially with digital logic circuits and MOS devices. It is also assumed that the servicing technician has the equipment, prints and tools required to properly service the Master Component.

The guide was developed to allow the servicing technician to repair the Master Component efficiently. The first causes listed are either the most common causes of the problems or causes that can be corrected with the Master Component assembled. After gaining experience servicing the MATTEL INTELLIVISION MASTER COMPONENT, the service technician should be able to identify and correct problems without using the troubleshooting guide.

SUBSTITUTION SEQUENCE OF PLUG-IN ICs ON PCB-LOGIC

	Symbol No.	Manufacturer's Type No.	Function	Part No.
1.	U2	RA-3-9600	SYSTEM RAM	(0098-0530)
2.	U4	AY-3-8900-1	STIC	(0098-0640)
3.	U1	CP-1610	CPU	(0098-0620)
4.	U9	RO-3-9502-011	PROGRAM ROM	(0098-0670)
5.	U3	RO-3-9504-021	PROGRAM ROM	(0098-0620)
6.	U5	RO-3-9503-003	GRAPHICS ROM	(0098-0570)
7.	U6	AY-3-8914	SOUND (PSG)	(0098-0660)
8.	U10	AY-3-8915	COLOR	(0098-0680)

- Always use a known-good IC.
- Always follow proper procedures and precautions for handling MOS devices.
- Be sure of correct IC orientation and pin insertion.
- Change only one IC at a time and leave in the known-good IC until the faulty IC is found.

SYMPTOM	SUSPECT	REMEDY
Snow on TV (with or without diagnostic test pattern visible)	The TV channel and Master Component channel selector switch do not agree.	Set the TV VHF channel switch and Master Component channel selector switch to the same channel.
	The Master Component is not energized.	Ensure the Master Component is connected to a 120V AC 60Hz power source and the ON/OFF switch is on.
	The antenna selector switch is not set to "GAME" or is defective.	Set the switch to "GAME" or replace if required.
	The coaxial RF cable is not connected properly or is defective.	Connect the cable correctly or replace.
	Solder bridges or foreign materials are causing shorts.	*Inspect for solder bridges or foreign materials in the Master Component.
	The Modulator PCB-LOGIC is defective.	*Connect a known-good modulator in parallel with the modulator. Connect the RF cable to the known-good modulator and touch the cases together. If this clears the problem, replace the modulator.
	* The modulator VCC is not +6V DC.	*Troubleshoot the VCC line.
	The +12V DC supply is defective.	*Troubleshoot the +12V DC supply and distribution systems on the PCB-Power Supply and PCB-LOGIC.
	The transformer or power switch assembly is defective.	*Troubleshoot the assembly for opens and shorts.
Grey-white screen with NO flash observed on the TV screen when the reset switch is depressed.	The STIC IC (U4) VCC jumper wire is disconnected from the PCB-Power Supply.	*Reconnect the jumper wire.
	The clock pulse circuit is not functioning.	*Troubleshoot the clock pulse circuit using the following as a guideline: 1) Substitute STIC IC (U4) with a known-good IC. 2) Substitute the Color IC (U10) with a known-good IC. 3) Check for the following voltages on the STIC IC (U4): Pin 40 = +5.5V DC, Pin 20 = -2.1V DC. 4) Check for +5V DC on Pins. 13. 16 and 17 of U10 (Color IC). 5) Check for ground on Pins 1 and 17 of U4 and Pin 1 of U10. 6) Check the PCB-LOGIC clock pulse circuits for opens and shorts. 7) Check capacitors C1 and C2 on the PCB-LOGIC. 8) Replace Crystal X1 on the PCB-LOGIC.
	Solder bridges or foreign material causing shorts on the PCB-LOGIC.	*Remove any foreign materials or solder bridges.

*Requires disassembly of Master Component to effect repair.

SYMPTOM	SUSPECT	REMEDY
Grey-white screen **WITH** flash occurring on the TV screen when the reset switch is depressed.	The test cartridge is incorrectly inserted into the Master Component.	Insert the cartridge correctly.
	The Master Component cartridge socket is defective.	Visually inspect the socket for bent pins, foreign material, etc.
	Defective test cartridge. No clock pulses or incorrect clock pulses at PCB-LOGIC IC U1 (CPU) Pins 37 and 38.	Try another cartridge. *Check for 3.3V DC drop across PCB-LOGIC zener diode CR2. Check for +16V DC at the junction of PCB-LOGIC resistors R2 and R16. Check pins 1 and 3 of IC U11 for clock pulse input. If no input, replace STIC IC (U4) on PCB-LOGIC. Check diodes CR3 and CR4. On PCB-LOGIC check zener diode CR5. On PCB-LOGIC check transistors Q1 and Q2. If IC U11 has clock input on pins 1 and 3 but no output on pins 2 and 4 and the discrete components are OK, replace U11.
	+5V DC supply problems.	*Troubleshoot +5V DC supply and distribution path.
	A defective plug-in IC on the PCB-LOGIC.	*Troubleshoot the plug-in ICs using the recommended sequence at the beginning of this chart. Observe insertion and removal precautions.
	A soldered-in IC is defective.	*Check the truth table for each IC. A problem with ICs U13 or U16 can be determined by removing ICs U2, U3, U5, U6, U9 and the test cartridge. If a LOGIC 1 is then measured at pin 6 of U13, then the problem is in either a defective U13 or U16.
	The PCB-LOGIC bus control signals are not functioning when checked at Pins 3, 4 and 5 of IC U1 (CPU).	*Using the circuit schematic, check all supply voltages for U1 (CPU) and U2 (SYSTEM RAM).
	Solder bridges or foreign materials causing shorts.	*Inspect the Master Component PCBs and circuits for foreign material or solder bridges.
Incorrect, extra, or missing video patterns or characters	One or more ICs are defective on the PCB-LOGIC	*Test the SYSTEM LOGIC using the MTE 201 diagnostic test. Replace PCB LOGIC ICs as required. Re-perform the diagnostic test to verify the failed IC. Most of the graphic problems are caused by PCB-LOGIC ICs U2, U4, U5, U7 and U8.
	The DC Power Supply is defective.	*Check all Power Supply voltages on both the PCB-LOGIC and PCB-Power Supply.
	Solder bridges or foreign material causing shorts.	*Inspect the PCB-LOGIC for foreign material or solder bridges.
	The test cartridge is defective.	Try another cartridge.

*Requires disassembly of Master Component to effect repair.

SYMPTOM	SUSPECT	REMEDY
Distorted TV picture	Interference from a nearby operating television transmitter.	Switch the television and Master Component to the other channel and/or disconnect the antenna wire from the antenna switch box.
	The test setup is incorrect.	Check all television controls, check all test connections, check for agreement between the TV VHF channel selector and the Master Component channel selector.
	STIC IC (U4) or Color IC (U10) on PCB-LOGIC is defective.	*Check these ICs using the substitution method.
	Defective modulator on the PCB-LOGIC	*Connect a known-good modulator in parallel with the modulator. Connect the RF cable to the known-good modulator and touch the two modulator cases together. If the problem clears, replace the modulator.
	Solder bridges or foreign materials causing shorts.	*Remove any solder bridges or foreign materials.
No Sound (picture and video OK)	TV volume turned down.	Check the TV volume setting.
	Sound IC (U6) on PCB-LOGIC is defective.	*Check U6 by substituting IC with a known-good Sound IC.
	The modulator on the PCB-LOGIC is defective.	*First check the audio input lead on the modulator for signal. If signal is present, connect a known-good modulator in parallel with the modulator. Connect the RF cable to the known-good modulator and touch the two modulator cases together. Reset the PCB-LOGIC and restart the diagnostic test. If the sound is OK, replace the modulator.
	Defective audio discrete components on PCB-LOGIC.	*Troubleshoot the audio circuits on the PCB-LOGIC.
	Solder bridges or foreign material causing shorts.	*Remove any solder bridges or foreign materials.
Hand Controller malfunctions	The Hand Controller is defective.	*Substitute a known-good Hand Controller for the suspected Hand Controller and perform the Hand Controller test.
	The Sound IC (U6) is defective on PCB-LOGIC.	*Substitute a known-good U6.
	The 9 Pin connector from the Hand Controller or associated traces are defective.	*Check the 9 Pin connector and associated traces on PCB-LOGIC.
	Other PCB-LOGIC ICs are defective.	*Utilizing the substitution method, check ICs U4, U2, U1, U9 and U3. If several hand control test pattern numbers and letters are white and none of the previous steps corrects the problem, replace IC U12 on the PCB-LOGIC. If this does not correct the problem, replace IC U11.

*Requires disassembly of Master Component to effect repair.

SYMPTOM	SUSPECT	REMEDY
The picture suddenly goes blank during the diagnostic test.	The test cartridge is defective.	Try another cartridge. Also check the Master Component cartridge socket.
	One or more plug-in ICs are defective.	*Using the recommended substitution sequence, check the plug-in ICs.
	The PCB-LOGIC reset switch is defective.	*Check the reset switch.
	The PCB-LOGIC Power Ribbon cable is defective.	*Check the Power Ribbon cable for breakage, opens, etc.
	The PCB-LOGIC Crystal X1 is defective.	*Check the crystal by **GENTLY** tapping it and observing the picture.
	Foreign material is causing a short.	*Inspect the Master Component for foreign materials.
Picture action freeze-up	One or more of the plug-in ICs are defective.	*Using the **following** sequence, replace the following ICs using the substitution method: U1 (CPU), U4 (STIC), U2 (SYSTEM RAM), U9 (SYSTEM ROM) and U3 (PROGRAM ROM).
	The test cartridge is defective.	Try another cartridge.
	The Master Component cartridge socket is defective.	Inspect the cartridge socket for bent pins, foreign materials, etc.
PCB-LOGIC channel selector switch does not operate correctly.	The switch is defective.	*Repair or replace the switch as required.
	The modulator is defective.	*Check the modulator on the PCB-LOGIC.
The picture has the wrong colors or no color.	The TV controls are set wrong.	Check all TV controls.
	The test connections are making poor contact.	Check all test connections.
	The crystal (X1) is at the wrong frequency.	*Check the frequency at PCB-LOGIC IC U4 (STIC) Pin 15. It should be 3,579,545 ± 100 Hz. Adjust the frequency by adjusting the variable capacitor (C2).
	STIC IC (U4) or Color IC (U10) is defective.	*Check U4 and U10 using the substitution method.
	Solder bridges or foreign material causing a short.	*Remove any solder bridges or foreign material.

*Requires disassembly of Master Component to effect repair.

SECTION 3
DISASSEMBLY

3.1 GENERAL. Before disassembly of the Master Component, perform the testing procedures detailed in Section 2 to determine the most likely cause of the malfunction. Disassemble the Master Component only to the extent necessary to accomplish repairs.

3.2 The following paragraphs provide procedures for complete disassembly of the Master Component. Modify the procedures as necessary to accommodate the extent of disassembly required. Disassembly procedures are keyed to the exploded view illustrations in Section 6 (Page 6-3).

WARNING

MAKE SURE THAT THE MASTER COMPONENT IS UNPLUGGED FROM THE POWER SOURCE BEFORE DISASSEMBLY. REMOVE THE CARTRIDGE FROM THE SOCKET AND DISCONNECT THE RF CABLE FROM THE MODULATOR OUTPUT JACK.

NOTE

Disassemble the Master Component in a clean, well-illuminated area.

3.3 DISASSEMBLY OF CONSOLE ASSEMBLY. Refer to Figure 6-1 (Page 6-3) and disassemble the console assembly as follows:

a. Remove six Phillips-head screws (1) securing top housing assembly (8) to bottom housing assembly (21). Avoid damaging the Hand Controllers when turning the Master Component over to remove the screws.

b. Remove power ON/OFF knob (4) from top housing (8) by gently pulling cap upward.

c. Lift top housing (8) off bottom housing assembly. Slide hand controllers (11) through openings in top housing.

d. It is not necessary to remove inlays (2, 3), fastener (5), reset button (6) or spring (7) from top housing (8) unless replacement is required.

e. Remove six screws (9) securing tray (10) to bottom housing assembly and remove tray. Keep the tray screws separated from the housing screws because they are different sizes.

f. Carefully disconnect the 5-pin ribbon cable (42, Figure 6-3) and 2-pin connector (58) from the power supply board assembly (14, Figure 6-1).

g. Lift the logic board assembly (12) straight up out of the bottom housing assembly. Carefully disconnect the hand controller assemblies (11) from the logic board assembly, noting position of hand controller connectors and routing of cables for proper reassembly.

h. Disconnect the 5-pin connector (17) from the power supply board assembly (14).

i. Remove two screws (13) securing the power supply board assembly (14) to the bottom housing assembly. Remove the power supply board assembly and insulator (15).

j. Remove four screws (16) securing transformer/switch assembly to bottom housing assembly. Note routing of wiring for proper reassembly, and remove transformer/switch assembly. Do not separate transformer (19), switch (18) and connector (17) unless replacement of component is necessary (refer to Section 4).

3-4. DISASSEMBLY OF HAND CONTROLLERS. Refer to Section 4-2 for disassembly and component replacement instructions on Hand Controllers.

DISASSEMBLY NOTES

SECTION 4
REPAIR, REPLACEMENT AND ADJUSTMENT

4.1 GENERAL. The following paragraphs provide procedures for repairing defective assemblies, replacing defective components, and performing circuit adjustments

4.2 HAND CONTROLLERS.

IMPORTANT: Make sure foreign material . . . dirt, dust, etc., does not come in contact with the circuit matrix or other plastic parts.

Unplug Master Component from power source. Disconnect switch box cable.

a. Disassembly: Turn the Hand Controller upside down on a flat surface and hold it firmly. Use a Phillips-head screw driver to remove the 4 screws. Remove bottom screws first. Set all 4 screws aside in a safe place. Refer to Figure 4-1 below.

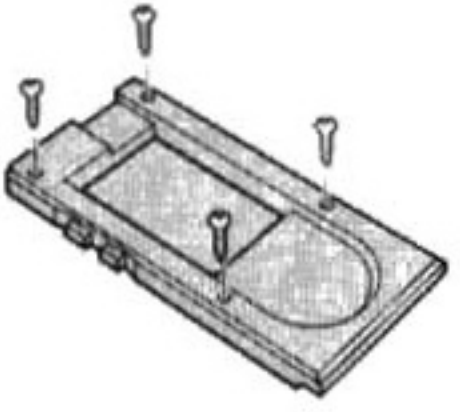


Figure 4-1

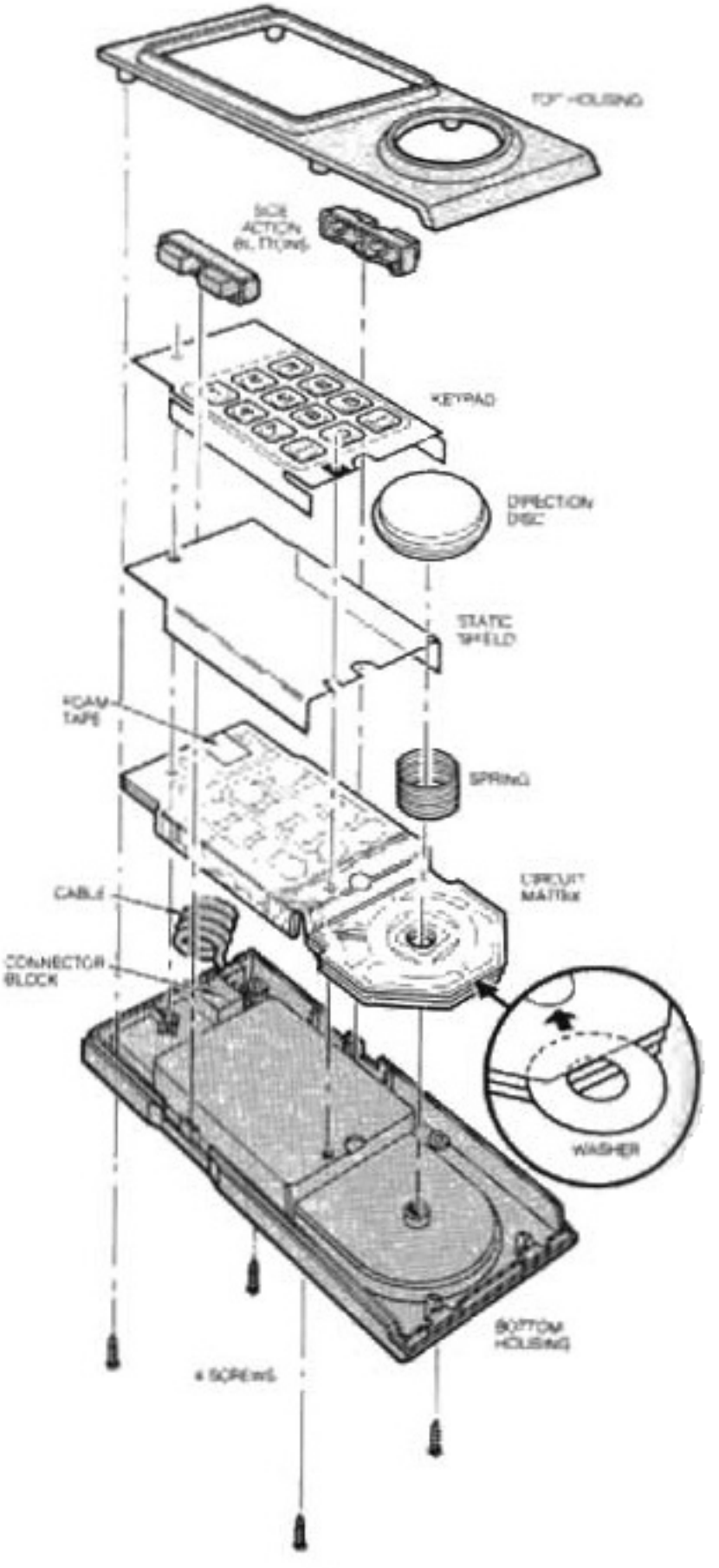


Figure 4-2

1) While holding the top and bottom housings together, turn the Hand Controller right side up. Set it back on a flat surface. (See Figure 4-3.)

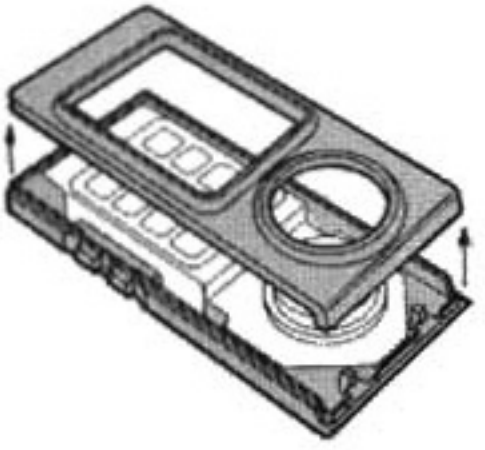


Figure 4-3

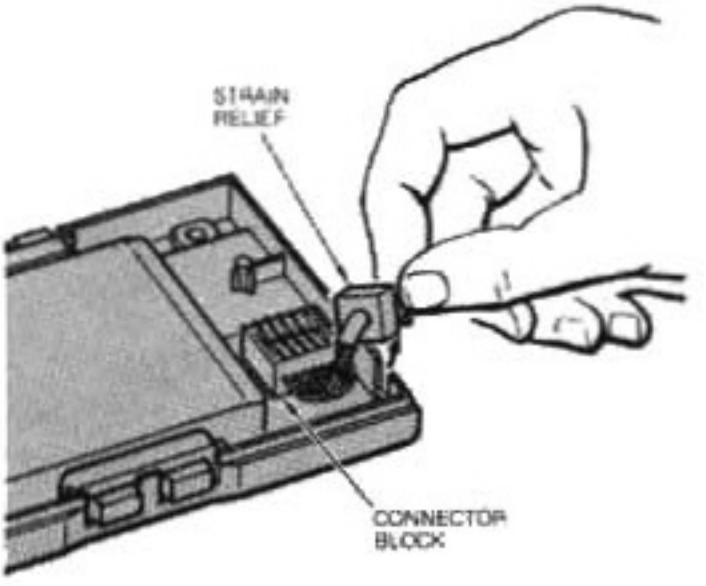


Figure 4-4

2) Carefully lift the top off and set it aside. Hold the number keypad and the Gold Directional Disc in place with one hand.

3) Remove the Gold Directional Disc and Spring.

4) Remove the Action Buttons from both sides.

5) Remove the static shield and the circuit matrix from the lower housing. (See Figure 4-2.)

6) Remove the cable from the lower housing by lifting the cable strain relief up and out of the housing. Pry up the cable connector block from its mount in the housing. **CAUTION:** Be careful not to touch or bend the metal prongs. (See Figures 4-4 and 4-5.)

7) If bottom housing has a raised lip around the directional disc guidepost, replace the bottom housing.

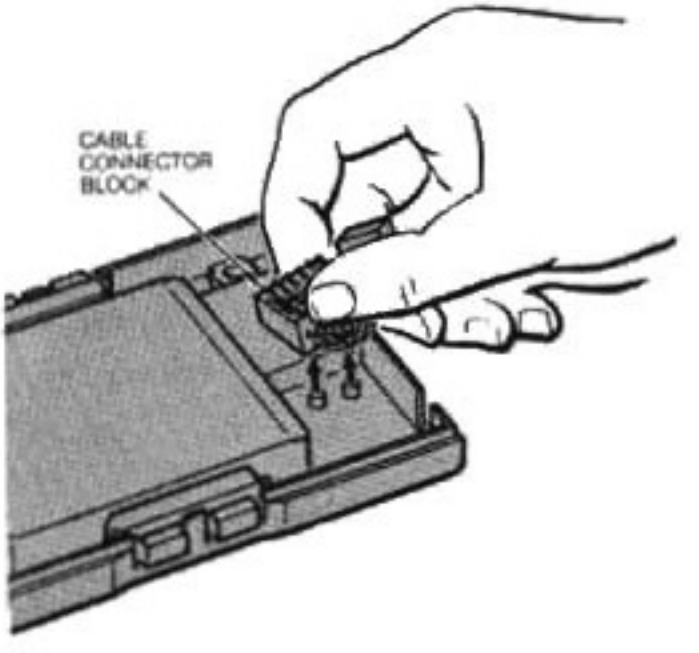


Figure 4-5

b. Component Replacement and Reassembly.

1) Place the replacement cable assembly in the lower housing as shown in Figure 4-4 and 4-5.

2) Make sure the replacement circuit matrix is correctly folded as shown in Figure 4-6 below.

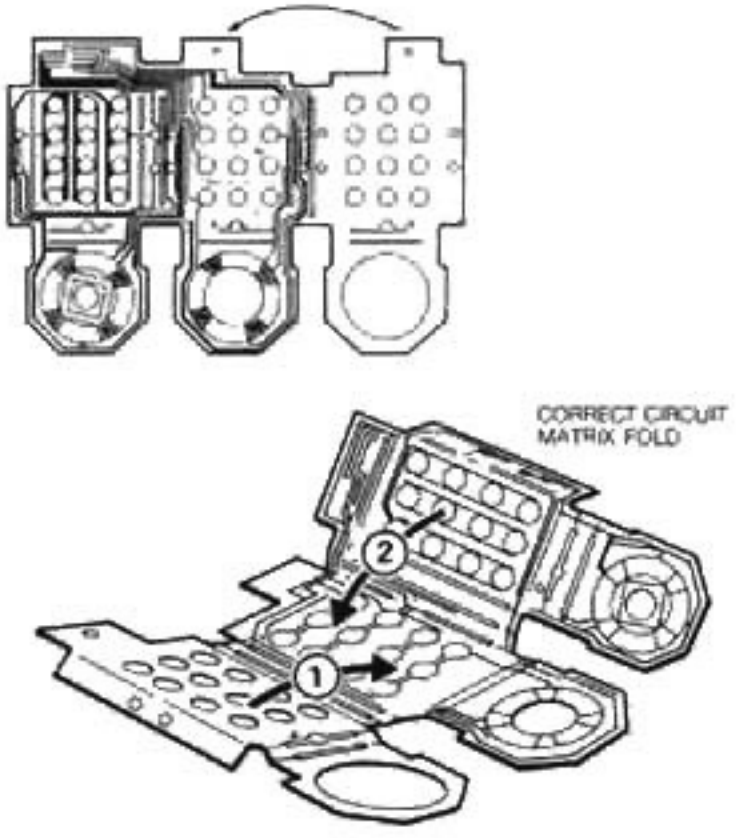


Figure 4-6

CAUTION: AVOID EXCESSIVE FOLDING OR HANDLING OF THE CIRCUIT MATRIX.

Apply foam tape (2609-6159) to circuit matrix as required Refer to Figure 4-7. Install the circuit matrix as shown in Figure 4-2 and make sure it fits snugly over the top and bottom posts.

Foam tape is to be applied directly to the folded circuit matrix. Tape is to be captured between matrix and domed legend, and pressed to secure its position. Refer to Figure 4-7.

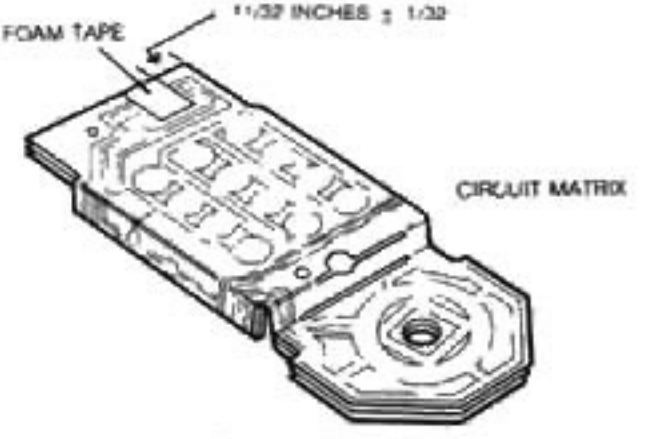


Figure 4-7 Foam Tape Replacement

3) Install the static shield over the folded circuit matrix, making sure the posts go through both sets of holes (shield and matrix). Refer to Figure 4-2. Hold the matrix and shield in place with fingers.

4) Install the keypad over the matrix and static shield. Again make sure both posts go through keypad holes.

5) Check that the components are correctly installed. Place the washer under the top layer of the circuit matrix and over the directional disc post as shown in Figure 4-2.

6) Press action buttons firmly in position. The scalloped edge should be on the BOTTOM, FACING INWARD. The buttons will only fit one way. Refer to Figure 4-8 below.

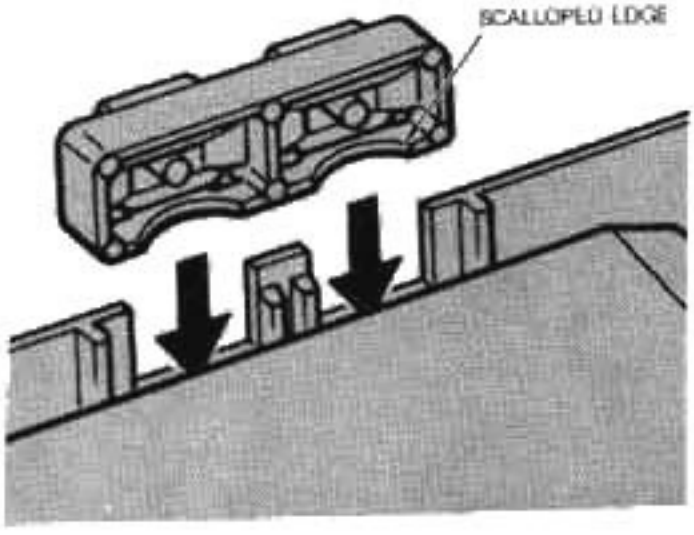


Figure 4-8

7) Mount the spring and Directional Disc. Refer to Figure 4-2.

8) Before reinstalling the top housing, make sure the circuit matrix and keypad are securely in place so that the top and bottom holes fit over the small brown posts. See Figure 4-9.

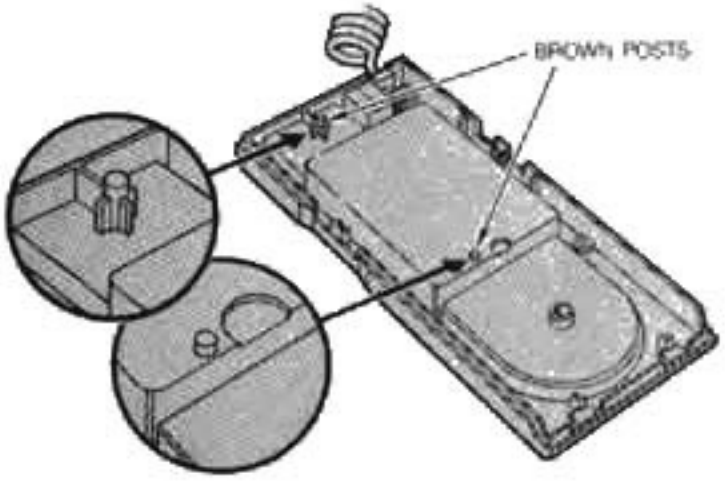


Figure 4-9

9) Install the top housing. Hold the top and bottom securely together while you turn the Hand Controller over. Replace the 4 screws, TOP SCREWS FIRST. Tighten until firmly in place. This is important to make all the circuit connections. DO NOT OVERTIGHTEN.

10) Connect the Hand Controller to a working M/C and using the MTE-201 Test Cartridge, check for proper operation.

4-3. LOGIC BOARD ASSEMBLY.

(1) Refer to Figure 4-10. Carefully unsolder and remove logic board shields. **NOTE: WHEN UNSOLDERING THE SHIELDS, BE SURE THAT EXCESS SOLDER DOES NOT CAUSE ANY SHORTS ON THE LOGIC BOARD COMPONENTS AND TRACES.**

(2) Inspect circuit board for evidence of broken or peeling circuit traces

(3) Inspect components on circuit board for evidence of charring, swelling, arcing or shorting.

(4) Inspect connectors for bent, broken or missing connector pins.

(5) Make sure all socket mounted ICs are fully seated in sockets. Make sure that heatsinks on ICs U1, U2 and U4 are securely attached to the ICs.

(6) Inspect all jumper wires for evidence of burned or frayed insulation. Make sure all jumper wires are securely soldered to circuit board.

(7) Make sure that connector J5 is securely attached to wire.

4.4 POWER SUPPLY BOARD ASSEMBLY.

(1) Inspect circuit board for evidence of broken or peeling circuit traces.

(2) Inspect components on circuit board for evidence of charring, swelling, arcing or shorting.

(3) Inspect connectors for bent, broken or missing connector pins.

(4) Make sure heat sinks are securely attached to voltage regulators U1 and U2.

(5) Make sure that adhesive holding capacitors C1 and C2 in position has not separated.

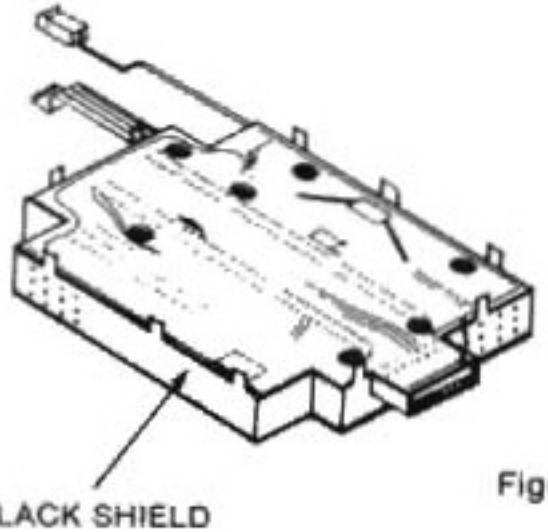
4-5. REPAIR. Repair the Master Component in accordance with the following procedures.

a. Transformer On/Off Switch Assembly Repair. Repair of the transformer on/off switch assembly consists of replacing either the switch or the transformer.

(1) Refer to Figure 4-11 for proper wire color and connections.

(2) Replace any transformers with damaged wire insulation.

(3) Replace defective On/Off switch utilizing a low wattage soldering iron.



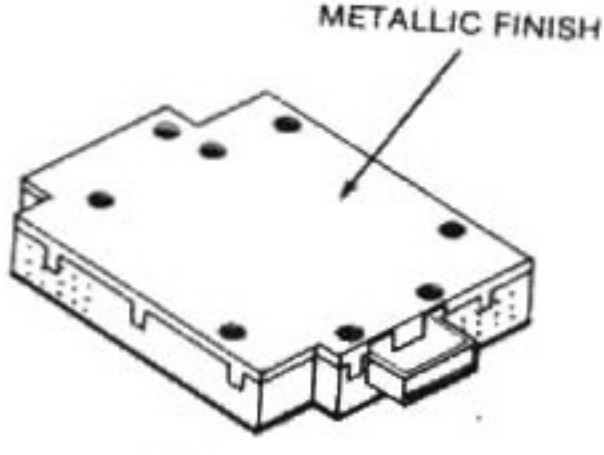
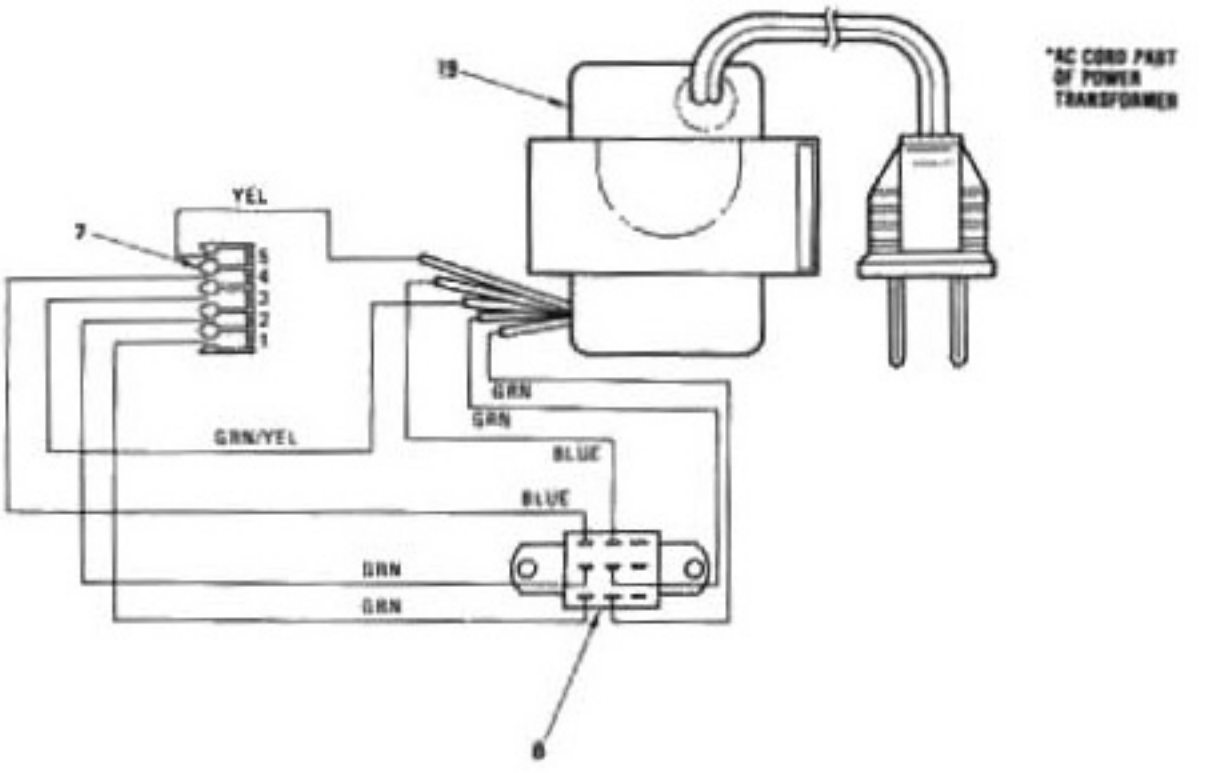


Figure 4-10



NOTES: 1 (INDEX) NUMBERS REFER TO FIGURE 6-1.
2 ALL WIRES ARE 22 AWG INSULATED WIRE.

Figure 4-11 Transformer ON/OFF Switch Wiring Assembly

b. Printed Circuit Board Repair. The following general procedures and precautions apply to repair of printed circuit boards.

(1) Many of the integrated circuits contained on the printed circuit boards are of MOS construction which are easily damaged from static discharge. To prevent damage due to static discharge, the following precautions should be observed:

a) All working surfaces must be at ground potential.

b) Use a low wattage (25 to 40 watt) grounded tip soldering iron.

c) ***Repair personnel should take necessary antistatic precautions such as the wearing of ground straps.***

(2) Support the circuit board so that it will not move or cause the soldering iron to strike other components.

(3) Install new components in the same position as they were removed.

(4) Inspect and test all resoldered connections.

(5) Use desoldering equipment, such as a solder vacuum, when unsoldering components.

(6) Use a heat sink on semi-conductor leads when soldering or unsoldering in the area.

(7) Remove excess solder, solder splatter and rosin splatter after repairs are completed.

(8) Remove socket mounted ICs by carefully prying out of socket with a small screwdriver.

(9) Install socket mounted ICs by bending IC pins into position over socket holes, and applying firm, even pressure to IC.

(10) Replace jumper wires with wire of the same gage.

(11) Reinstall logic board shields as illustrated in Figure 4-10.

4-6. REPLACEMENT.

a. Replace all components and assemblies which are damaged beyond repair.

b. Install new heatsinks on voltage regulators in accordance with paragraph 4-6.d.

c. Install heatsinks on new ICs U1, U2 and U4 in accordance with paragraph 4-6.e.

d. Regulator/Heatsink Assembly Replacement. Install voltage regulators on heatsinks as follows (PCB-POWER SUPPLY):

(1) Remove defective regulator from heatsink by removing eyelet or screw. Pry defective regulator off.

(2) Clean dried thermal compound off of heatsink.

(3) Apply an even coat of general purpose thermal compound on contact surface of regulator.

(4) Position regulator in place on old heatsink. Secure regulator to heatsink with a suitable screw and nut. Regulator must be secured tightly to heatsink surface to insure maximum heat transfer.

e. Integrated Circuit Heatsink Replacement. Install integrated circuit heatsinks on ICs U1, U2 and U4 as follows (LOGIC BOARD):

(1) Remove heatsink from defective IC by prying off. Application of heat from heat gun may be required to remove heatsink.

(2) Remove dried thermal bonding compound from heatsink. (NOTE: May have to heat heatsink to remove.)

(3) Apply an even coat of thermally conductive epoxy on IC.

(4) Place heatsink on IC and apply sufficient pressure to ensure bonding.

4.8 ADJUSTMENTS.

a. Master Clock Adjustment.

(1) Connect a frequency counter with a high input impedance to pin 10 of J1 (cartridge jack) and ground or pin 15 of IC U10 and ground.

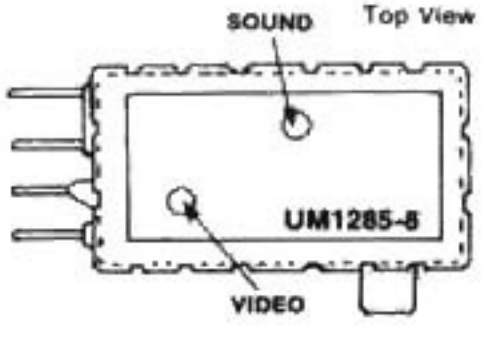
(2) Adjust C2 (variable capacitor) so the frequency counter indicates 3.579545 MHz ± 100 Hz.

b. Sound Buzz Adjustment.

(1) With the volume on the television adjusted for normal listening level, no sync. buzz should be heard.

(2) If a buzz is heard, adjust the sound coil on the RF modulator for minimum buzz. CAUTION: Use care not to damage the core of the sound coil.

(3) If the buzz cannot be reduced to a satisfactory level, replace the modulator (2609-4689).



RF Modulator
(2609-4689)

SECTION 5
ASSEMBLY

5-1. GENERAL. The following paragraphs provide procedures for assembly of the Master Component. Assembly procedures are keyed to the exploded views in Section 6.

5-2. ASSEMBLY OF CONSOLE ASSEMBLY. Refer to Figure 6-1 (Page 6-3) and assemble the console assembly as follows:

a. If disassembled, reassemble transformer (19), switch (18), connector (17) and associated wiring in accordance with Figure 4-11 and Wiring Diagram (Figure 5-2).

b. Install transformer/switch assembly in bottom housing (21). Route wiring as noted during disassembly. Secure assembly in place with four screws (16).

c. Install insulator (15) in bottom housing. Install PCB-Power Supply (14) on insulator in bottom housing assembly. Secure PCB Power Supply to bottom housing with two screws (13).

d. Connect the 5-pin connector (17) from the transformer/switch assembly to the PCB Power Supply (14) as illustrated in Figures 5-1 and 5-2.

e. Connect the hand controller assemblies (11) cable connector to the PCB Logic (12) as illustrated in Figures 5-1 and 5-2. Route hand controller cables in bottom housing assembly (21) as noted during disassembly. Place the PCB Logic in bottom housing assembly.

f. Carefully connect the 5-pin ribbon cable (42, Figure 6-3) and 2-pin connector (58) from the PCB Logic (12, Figure 6-1) to the PCB Power Supply (14) as illustrated in Figures 5-1 and 5-2.

g. Install tray (10) in bottom housing assembly (21) and secure in place with six screws (9).

h. If removed, install spring (7), reset button (6) and fastener (5) on top housing assembly (8).

i. Slide hand controller assemblies (11) through openings in top housing assembly (8). Install top housing assembly on bottom housing assembly (21).

j. Install glamour cap (ON/OFF knob). Press firmly into place.

k. Carefully invert console assembly and secure top housing assembly (8) to bottom housing assembly (21) with six screws (1).

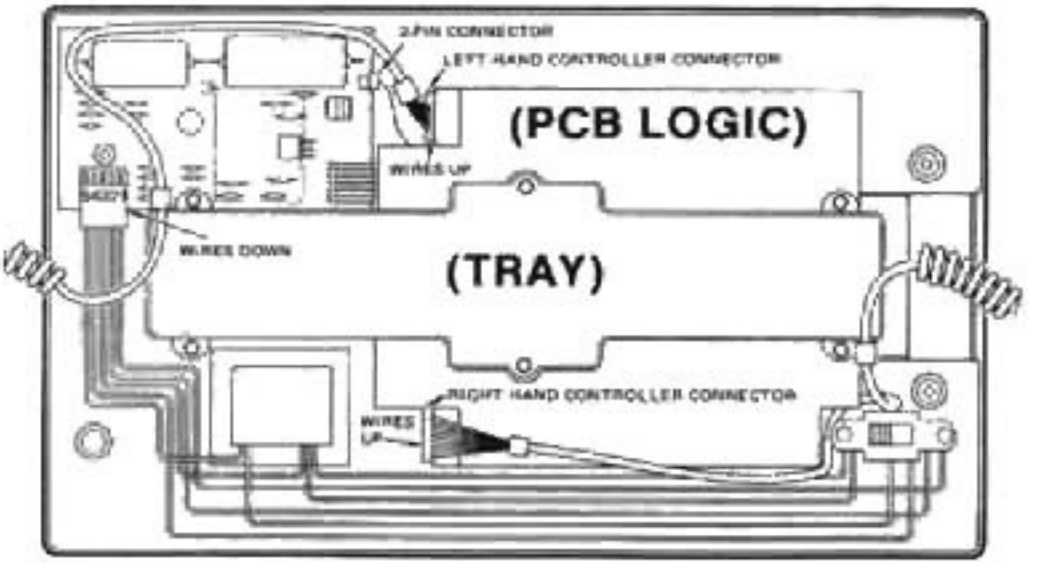
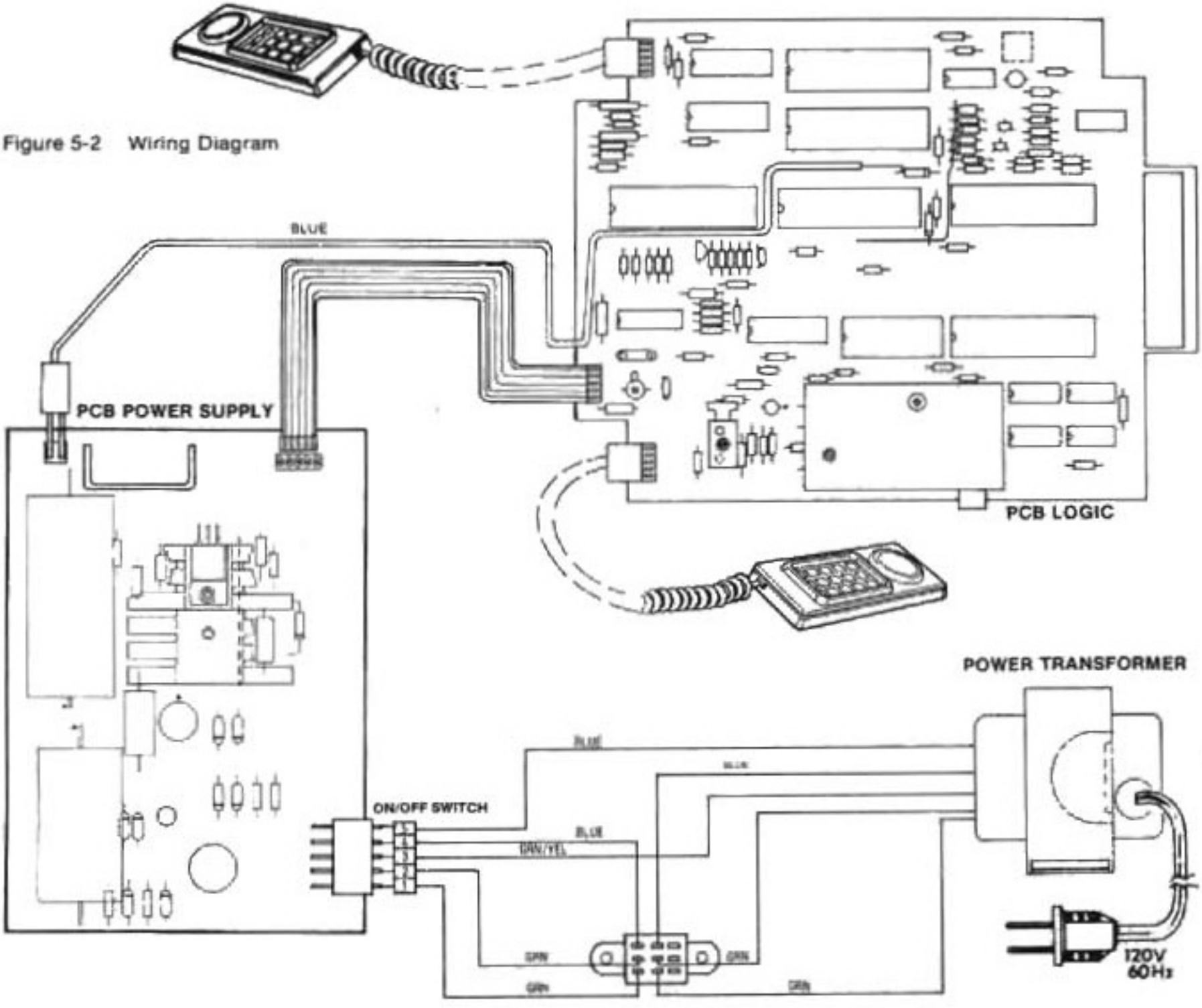


Figure 5-1 Connector Installation Diagram

Figure 5-2 Wiring Diagram



SECTION 6
PARTS LIST

6-1. HOW TO USE THE PARTS LIST.

a. PARTS IN SHADED AREA AND MARKED WITH⚠HAVE SPECIAL CHARACTERISTICS TO MAINTAIN THE SAFETY PERFORMANCE OF THIS UNIT. WHEN REPLACING ANY OF THESE PARTS, BE SURE TO USE ONLY THOSE SPECIFIED PARTS.

b. Locate the desired part on Figures 6-1 through 6-4 and note the numerical index number or reference designator of the part, as applicable.

c. Find the index number or refrence designator in the associated detailed parts index.

d. Order replacement parts by part number with complete description from Mattel Electronics Parts Department.

NOTE

EQUIVALENT COMMERCIAL ITEMS MAY BE SUBSTITUTED FOR MATTEL COMPONENTS WHICH HAVE AN ASTERISK (*) FOLLOWING THEIR PART NUMBER.

6-2. DETAILED PARTS LIST. Replaceable parts and assemblies for the Mattel Intellivision Master Component are illustrated in Figures 6-1 through 6-4 and indentified by index number in the associated detailed parts lists.

6-3. ABBREVIATIONS. Abbreviations used in this parts list include:

Symbol/Abbreviation	Definition
AR	As required
ASSY	Assembly
*	Commercial items may be substituted for preceding part number
IN.	Inch
K	Thousand
NHA	Next higher assembly
Ω	Ohm
µF	Microfarads
pF	Picofarads
REF	Reference item; quantity indicated in first appearance
V	Volts
W	Watt
W/W	Wire Wound

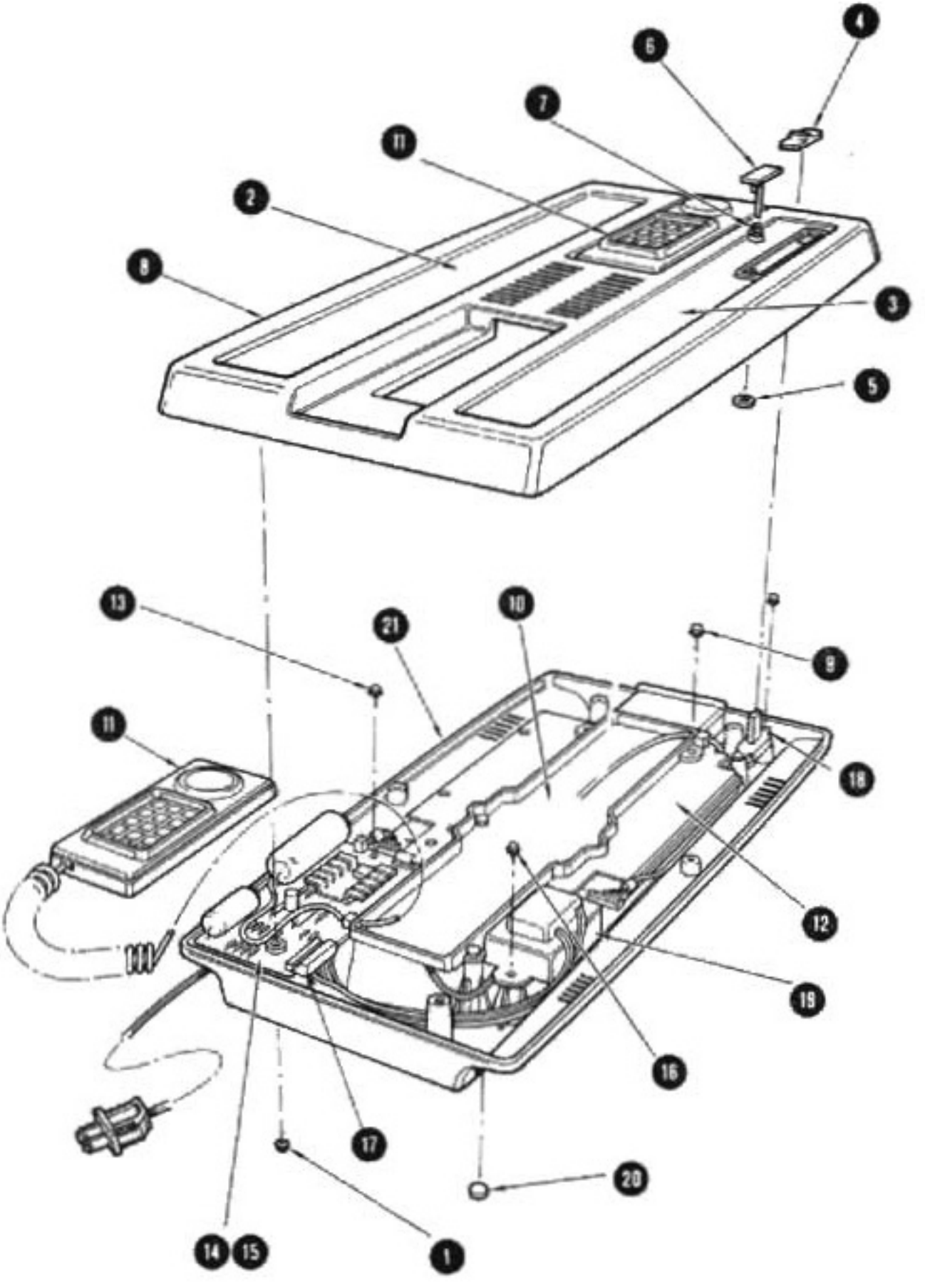


Figure 6-1 EXPLODED VIEW . . . . . Console Assembly

Fig. & Index No.	Part Number	Description	QTY
6-1-		CONSOLE ASSY	REF
-1	0405-0832*	SCREW, 8-18 x 3/4 in.	6
	2609-9719	HOUSING ASSY, Top	1
-2	2609-4529	INLAY, Plain	1
-3	2609-4519	INLAY, Control	1
-4	2609-2139	GLAMOUR CAP (ON/OFF KNOB)	1
-5	0405-0582	FASTENER, Pushnut	1
-6	2609-2129	BUTTON, Reset	1
-7	2609-4269	SPRING, Reset button	1
-8	2609-6069	HOUSING, Top	1
-9	0405-0802*	SCREW, 8-18 x 3/4 in.	6
-10	2609-2149	TRAY	1
-11	2609-9059	HAND CONTROLLER ASSY (see Figure 6-2 for breakdown)	2
-12	2609-9169	LOGIC BOARD ASSY ⚠	1
-13	0405-0812*	SCREW, 8-18 x 1/2 in.	2
-14	2609-9539	POWER SUPPLY BOARD ASSY ⚠	1
-15	2609-0230	INSULATOR ⚠	1
-16	0405-0822*	SCREW, 6-19 x 1/2 in.	4
	2609-9629	TRANSFORMER/SWITCH ASSY ⚠	1
-17	2609-9229	CONNECTOR, 5-pin ⚠	1
-18	2609-9559	SWITCH, Slide ⚠	1
-19	2609-9549	TRANSFORMER ⚠	1
-20	2609-9489	FOOT, Adhesive	4
-21	2609-9739	HOUSING ASSY, Bottom	1

PARTS IN SHADED AREA AND MARKED WITH ⚠ HAVE SPECIAL CHARACTERISTICS TO MAINTAIN THE SAFETY PERFORMANCE OF THIS UNIT. WHEN REPLACING ANY OF THESE PARTS, BE SURE TO USE ONLY THOSE SPECIFIED PARTS.

HAND CONTROLLER ASSEMBLY

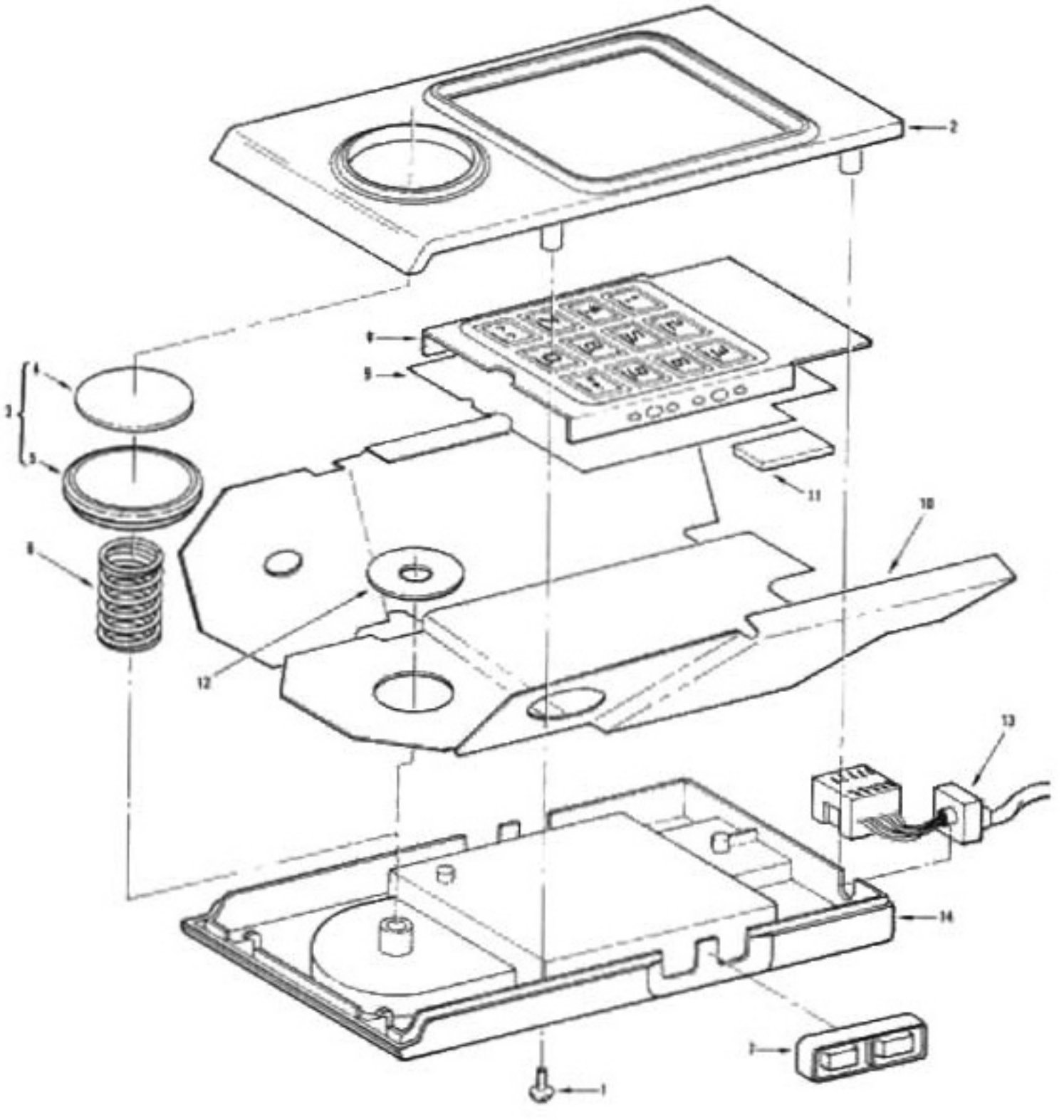


Figure 6-2

MISSING PARTS LIST!

MISSING FIGURE 6-3!

Fig. & Index No.	Part Number	Description	QTY
6-3-	2609-9169	LOGIC BOARD ASSY (see Figure 6-1 for NHA)	REF
-1	2609-4479	RF SHIELD, Top	1
-2	2609-4489	RF SHIELD, Bottom	1
-3	2609-9759	PLUG, 9-pin (P4A, P4B)	2
-4	0096-0070*	CAPACITOR, 0.01μF (C34 through C39)	6
-5	0085-1500*	CAPACITOR, 0.1μF, 25V, ±20% (C3, C4, C6 through C21, C23 through C25, C29, C32)	24
-6	0098-0590	INTEGRATED CIRCUIT (U7, U8, U12)	3
-7	0098-0570	INTEGRATED CIRCUIT (U5)	1
-8	0098-0640	INTEGRATED CIRCUIT (U4)	1
-9	0098-0530	INTEGRATED CIRCUIT (U2)	1
-10	0099-1030*	DIODE, 1N4001 (CR1, CR6, CR7)	3
-11	0095-0781*	RESISTOR, 1K, 1/4W, ±5% (R6, R17)	2
-12	0098-2110*	INTEGRATED CIRCUIT, 7407 (U11)	1
-13	0086-0426*	DIODE, Zener 10V (CR5)	1
-14	0099-1050*	DIODE, 1N4148 (CR3, CR4, CR8)	3
-15	0099-1140	SWITCH, Momentary contact (S1)	1
-16	0085-0007*	CAPACITOR, 1.0μF, 20V, ±20% (C26)	1
-17	0095-0961*	RESISTOR, 5.6K, 1/4W, ±5% (R4, R13, R18)	3
-18	0098-1100*	TRANSISTOR, 2N3906 (Q1, Q2)	2
-19	0099-1350	FERRITE BEAD (L1, L2)	2
-20	0095-0022*	RESISTOR, 10K, 1/4W, ±5% (R15)	1
-21	0086-0425*	DIODE, Zener 3.3V (CR2)	1
-22	0098-2640*	INTEGRATED CIRCUIT, 74LS86 (U17)	1
-23	0095-0541*	RESISTOR, 100Ω, 1/4W, ±5% (R16)	1
-24	0095-0501*	RESISTOR, 68Ω, 1/4W, ±5% (R2)	1
-25	0099-1360	FERRITE BEAD (L3)	1
-26	0098-0520	INTEGRATED CIRCUIT (U1)	1
-27	2609-9399	CONNECTOR, 44-pin (J1)	1
-28	0098-0670	INTEGRATED CIRCUIT (U9)	1
-29	0098-2600*	INTEGRATED CIRCUIT, 74LS27 (U13)	1
-30	0098-2520*	INTEGRATED CIRCUIT, 74LS00 (U16)	1
-31	0098-2120*	INTEGRATED CIRCUIT, 74LS125 (U14, U15)	2
-32	0095-0650*	RESISTOR, 300Ω, 1/4W ±5% (R23)	1
-33	2609-4689	RF MODULATOR	1

Fig. & Index No.	Part Number	Description	QTY
6-3-34	0098-0620	INTEGRATED CIRCUIT (U3)	1
-35	0095-0890*	RESISTOR, 3K, 1/4W, ±5% (R24)	1
-36	0085-0009*	CAPACITOR, 47μF, 16V, -10, +50% (C40)	1
-37	0095-0601*	RESISTOR, 180Ω, 1/4W, ±5% (R22)	1
-38	0089-0700	SWITCH, Channel select (S2)	1
-39	0084-0417*	RESISTOR, 22K, 1/4W, ±2% (R3, R10, R11)	3
-40	0085-0720*	CAPACITOR, 20pF, 15V, ±5% (C1)	1
-41	0099-0730	CAPACITOR, Variable (C2)	1
-42	0089-0472	RIBBON CABLE ASSY, 5-pin (P3)	1
-43	0089-0151	CRYSTAL (X1)	1
-44	0085-0722*	CAPACITOR, 220pF, 15V, 10% (C33)	1
-45	0095-0082*	RESISTOR, 18K, 1/4W, ±5% (R9)	1
-46	0084-0329*	RESISTOR, 2.7K, 1/4W, ±2% (R1)	1
-47	0098-0680	INTEGRATED CIRCUIT (U10)	1
-48	0085-0008*	CAPACITOR, 10 F, 20V ±20% (C27, C28, C30)	3
-49	0084-0361*	RESISTOR, 5.6K, 1/4W, ±2% (R14)	1
-50	0098-0170*	TRANSISTOR, 2N3904 (Q3)	1
-51	0084-0257*	RESISTOR, 470Ω, 1/4W, ±2% (R7)	1
-52	0084-0297*	RESISTOR, 1.2K, 1/4W, ±2% (R8)	1
-53	0095-0941*	RESISTOR, 4.7K, 1/4W, ±5% (R12)	1
-54	0084-0381*	RESISTOR, 9.1K, 1/4W, ±2% (R19)	1
-55	0084-0485*	RESISTOR, 110K, 1/4W, ±2% (R20)	1
-56	0085-0721*	CAPACITOR, 680pF, 15V, 20% (C31)	1
-57	0098-0660	INTEGRATED CIRCUIT (U6)	1
-58	0089-0008	CONNECTOR, 2-pin (J5)	1
-59	0099-1510*	SOCKET, 40-pin dip	6
-60	0099-1530*	SOCKET, 28-pin dip	1
-61	0099-1520*	SOCKET, 18-pin dip	1
-62	2609-4259	HEATSINK	3
-63	——	PRINTED CIRCUIT BOARD (Blank)	1

NOTES

SECTION 7
SCHEMATIC DIAGRAMS AND TECHNICAL INFORMATION

7-1. GENERAL. This section contains schematic diagrams illustrating the electronic circuitry of the Master Component. Technical data on the integrated circuits, RF modulator and power transformer is also contained in this section. The schematic diagrams and technical data should be used, as necessary, as an aid in troubleshooting and repairing the Master Component.

7.2. The following diagrams are contained in this section:

Figure 7-1. PCB-Power Supply
Figure 7-2. PCB-Logic

7.3. ABBREVIATIONS. Abbreviations used in schematic diagrams include:

Symbol/Abbreviation	Definition
BAR	Bus to Address Register
BC	Bus Control
BDIRIN	Bus Direction In
BDIROUT	Bus Direction Out
$\overline{\text{BDRDY}}$	Bus Data Ready
$\overline{\text{BUSAK}}$	Bus Acknowledge
CBLNK	Cartridge Blank
CLK	Clock
CS	Chip Select
DB	Data Bus
DTB	Data to Bus
DWS	Data Write Stop
$\overline{\text{ENAB}}$	Enable
$\overline{\text{INTR}}$	Interrupt
MCLK	Mast Clock
$\overline{\text{MSYNC}}$	Master Synchronization
$\overline{\text{OD}}$	Output Disable
PCIT	Program Counter Inhibit/Trap
$R/\overline{W}$	Read/Write
SD	Secondary Data
SR	Synchronization Register
STPST	Stop Start
V	Video
Y	Luminance

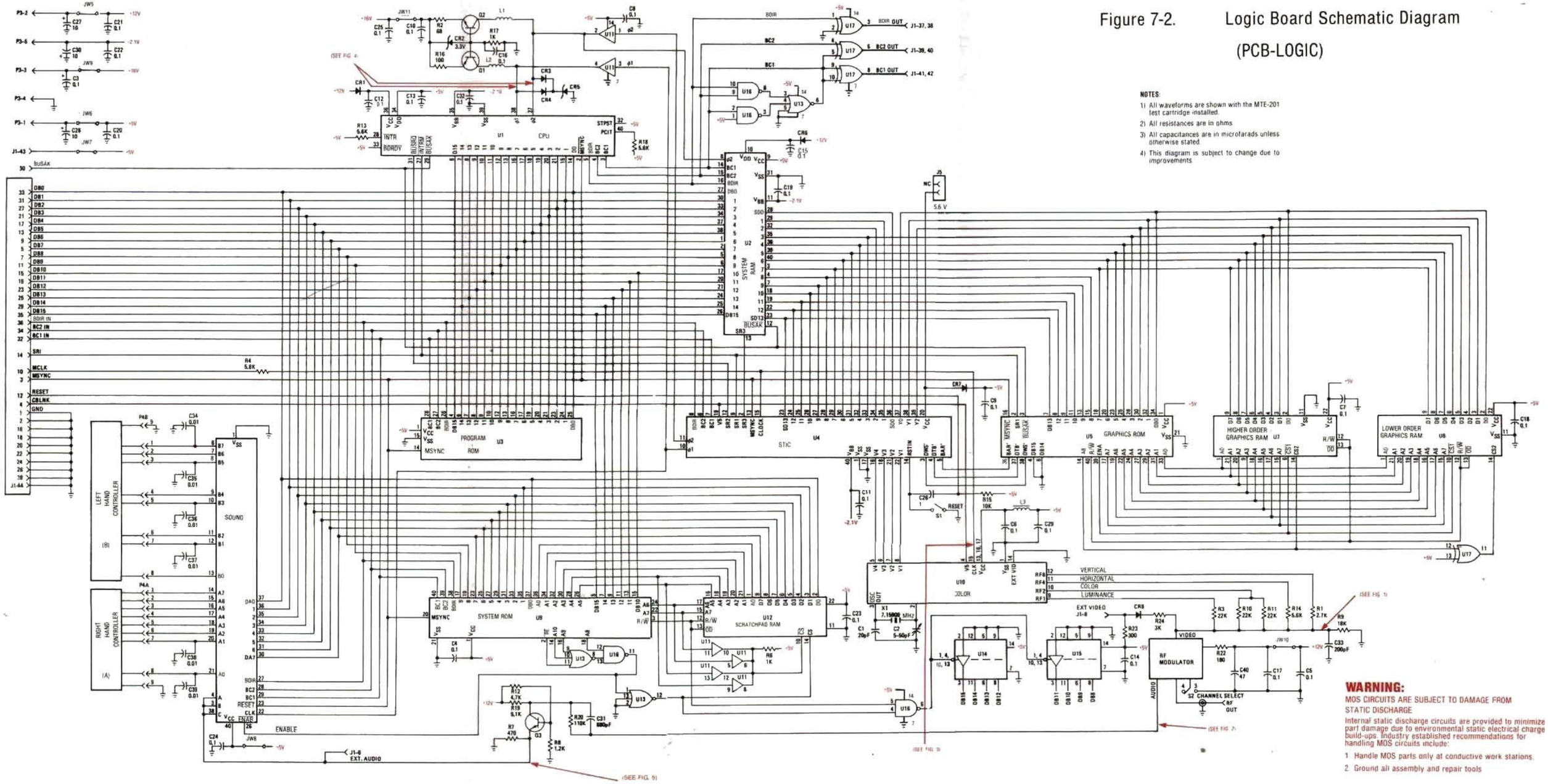


Figure 7-2. Logic Board Schematic Diagram

(PCB-LOGIC)

NOTES:

1) All waveforms are shown with the MTE-201 test cartridge installed.
2) All resistances are in ohms.
3) All capacitances are in microfarads unless otherwise stated.
4) This diagram is subject to change due to improvements.

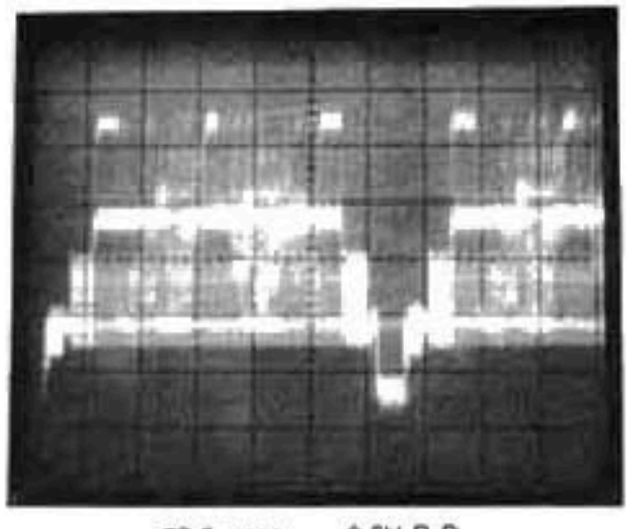
WARNING:

MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

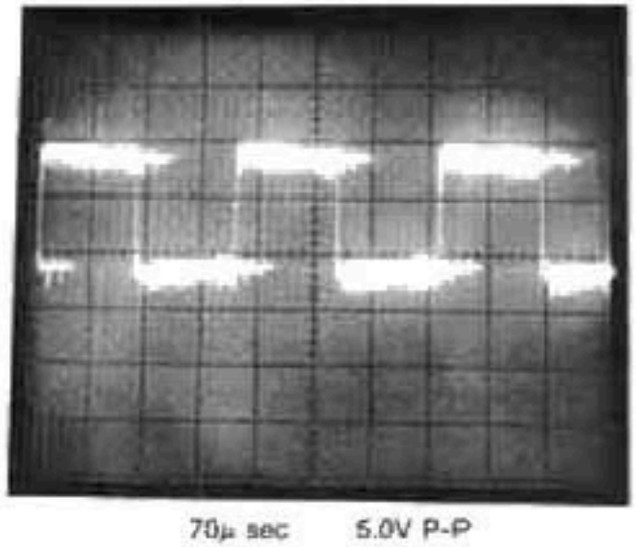
1. Handle MOS parts only at conductive work stations.
2. Ground all assembly and repair tools

Figure 1



63.5μ sec. 0.6V P-P

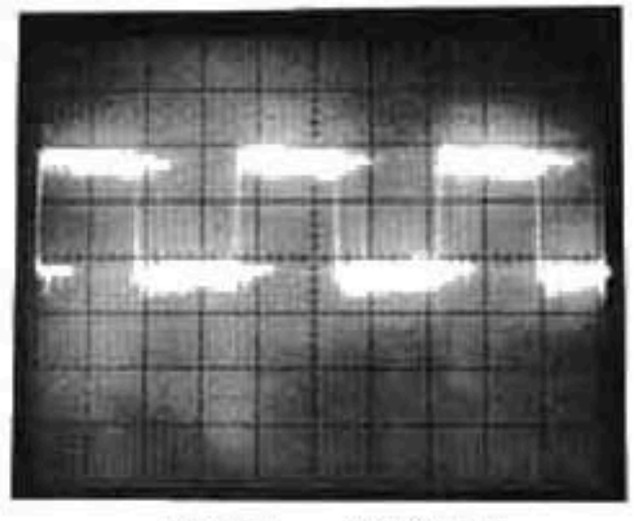
Figure 2



70μ sec 5.0V P-P

NOTE: Frequency and wave form will constantly vary with sound program.

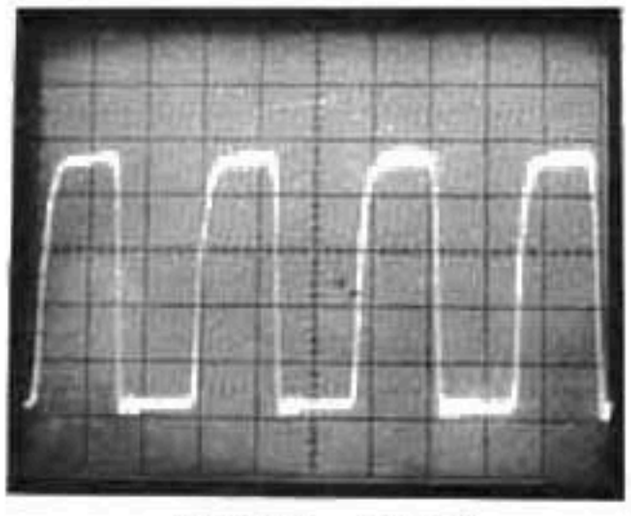
Figure 5



70μ sec 0.160V P-P

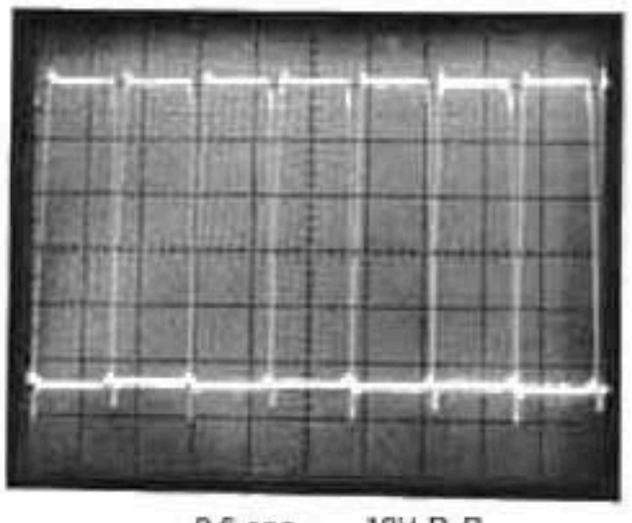
NOTE: Frequency and waveform will constantly vary with sound program

Figure 3



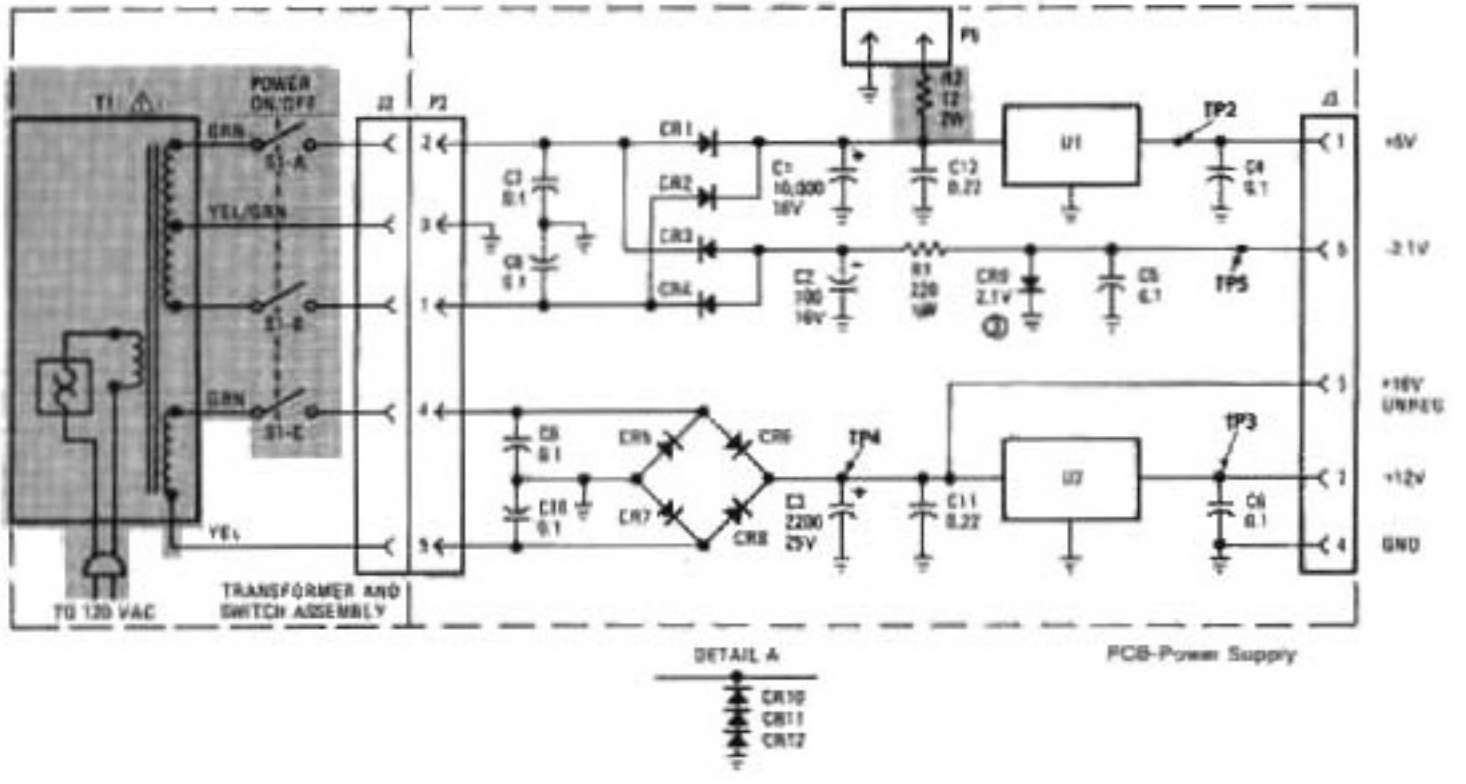
0.3 μ sec. 5.0V P-P

Figure 4



0.6 sec. 12V P-P

NOTE: Both waveforms are shown from pins 37 and 38 of U1 to illustrate 180° phase relationship. Individually, waveforms will appear identical.



NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. DIODES CR10 THRU CR12 MAY BE USED IN PLACE OF ZENER DIODE CR9 (SEE DETAIL A)
4. ALL VOLTAGES MEASURED WITH AN AC INPUT OF 120V 60Hz.
5. PARTS IN SHADED AREA AND MARKED WITH ⚠ HAVE SPECIAL CHARACTERISTICS TO MAINTAIN THE SAFETY PERFORMANCE OF THIS UNIT. WHEN REPLACING ANY OF THESE PARTS, USE ONLY THOSE SPECIFIED PARTS.

Figure 7-1 Power Supply Board Schematic Diagram (PCB-Power Supply)

TECHNICAL INFORMATION: CP-1610 (0098-0520) U1

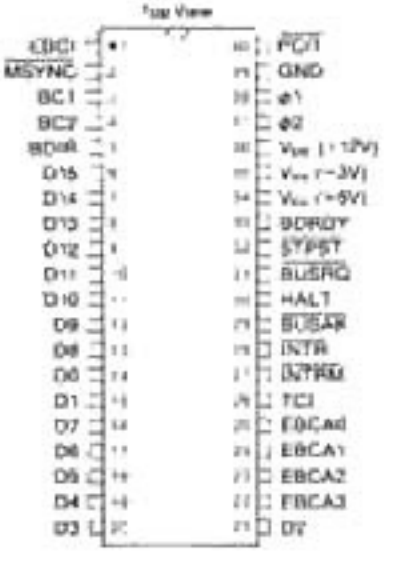
CP 1610*

16-BIT MICROPROCESSOR

FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2s complement arithmetic
- Status logic and word carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1610: 1μs cycle time, 2MHz 2-phase clock

Pin Configurations
40 Lead Dual In Line



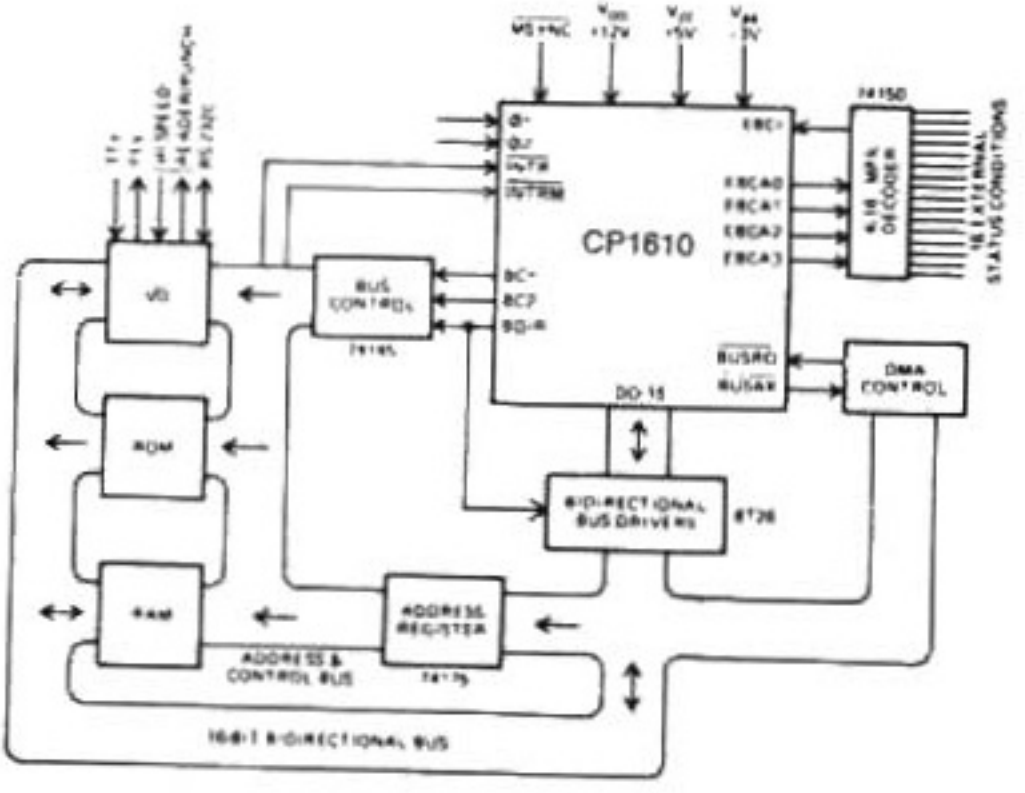
DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications. The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232-C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

*For more detailed data refer to General Instrument data specification book.



CP1610 SYSTEM DIAGRAM

TECHNICAL INFORMATION: RA—3-9600 (0098-0530) U2
RA-3-9600*

SYSTEM RAM

FEATURES

- Memory area 352 words of 16 bits
- Address counter and control logic for D.M.A. operation
- Control decoder for CPU data control signals
- Memory map comparator and control logic for additional memory on 14 bit bus
- Current line buffer — 20 words of 14 bits
- Drive capability on 16 bit and 14 bit bus for 1 TTL load and 100pF

FUNCTIONAL DESCRIPTION

The RA-3-9600 is a 'dual port' interface and 16 bit wide RAM storage area. The RA-3-9600 contains twenty 14 bit serial data buffer registers with separate bus control signals.

The RA-3-9600 memory is 352 x 16 bit contiguous words from address 512-863 with the graphics descriptors using the first 240 words. The graphics use only the lower 14 bits of each word leaving the two most significant bits available for user storage.

OPERATION DESCRIPTION

The RA-3-9600 RAM accepts data from the CPU via a 16 bit bi-directional bus which is time multiplexed with address and data. A 3 bit control bus from the CPU is used to provide strobe signals for the on-chip address latch and main memory area.

The RAM has two operating modes:

Mode 1—On decoding an interrupt the RAM is enabled into a bus copy mode. In this mode the RAM copies the lower fourteen bits of the CPU bus onto the graphics bus. The direction of copy is always from the CPU and towards the graphics except during a bus reversal condition. The reversal condition is indicated when the CPU requests a read from an external graphics address on the 14 bit bus. Under this condition the 9600 will turn its 14 bit bus outputs into tri-state and gate the 14 bits bus through to the 16 bit CPU bus.

Mode 2—is selected when the CPU issues BUSAK command (DMA request). The effect of BUSAK inside the 9600 is to reset the interrupt synchronizing logic and to switch the address decoder from the CPU address register to the graphics address counter. This counter, which sequences through the 240 words of graphics data, will have been previously set to zero when the interrupt signal was decoded. When the CPU is in the DMA state, the graphics system will prepare to display a new row of twenty characters and to load the 20 buffer registers within the 9600. For the first cycle of DMA after interrupt the graphics address counter will be at zero and the data at that address is passed to the 14 bit output. The action of SR3 will enable the output buffers and drive the 14 bit bus. The twenty shift registers are also loaded at this time. The negative edge of SR3 tri-states the 14 bit output and increments the graphics address counter. The shift registers are also clocked at this time. The SR3 input provides twenty positive pulses to the 9600 and loads the shift register buffers while giving the graphics the first row of characters. At the end of the first DMA cycle, after the CPU interrupt, the graphics address counter will be at value 20. The 9600 operation for the next fifteen lines will be to clock the 20 shift registers and gate the contents onto the 14 bit bus under control of the SR3 input. When the CPU is running and BUSAK is a logic 1, the graphics address counter is not incremented and it stays at the value 20. At the end of the first row of characters, the complete DMA opration is repeated and the address counter will be left at 40. This sequence occurs for the 12 rows of characters until all 240 have been successfully accessed.

The operation of SR3, INCREMENT/TRI-STATE signal, is to step the shift register sequentially through each of the twenty characters. If the BUSAK signal is low; i.e., in DMA, it also increments the graphics ADDRESS COUNTER. SR3 disables the 14 bit graphics bus during the low period.

At the end of active picture the STIC issues an interrupt request to the CPU. The RA-3-9600 tests for the INTAK* response from the CPU and uses this signal as an entry control for a copy mode between the two buses. The end of the copy mode is controlled by the first BUSAK negative edge.

*INTAK equivalent BC1, BC2, BDIR = 1.

Pin Configurations
40 Lead Dual In Line

*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: RO-3-9504 (0098-620) U3
RO-3-9504*

PROGRAM ROM

FEATURES

- Mask programmable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K Memory area
- 16 bit tri-state bus with higher 6 bits driven to zero during read operations

CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1610 microprocessor. It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

From initialization, the RO-3-9504 waits for the first address code; i.e., BAR. For this address code and all subsequent address sequences the 9504 reads the 16-bit external bus and latches the value into its address register.

The 9504 contains a programmable memory map location for its own 2K page, and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus.

INPUT CONTROL SIGNALS

BCIR	BCI	BC2	Equivalent Signal	Response
0	0	0	NACT	NACT
0	0	1	IAB	NACT
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB (READ)
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: RO-3-9503 (0098-0570) U5

RO-3-9503*

GRAPHICS ROM

FEATURES

- Mask programmable storage providing 2048 x 8 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K memory area
- 8 bit tri-state bus with higher 8 bits driven to zero during read operations
- 11 bit, static address outputs for external memory
- Control signals for external memory:
  $\overline{\text{ENABLE}}$
  R/$\overline{\text{W}}$
- Bus drive capability, 1 TTL load and 100pF plus tri-state

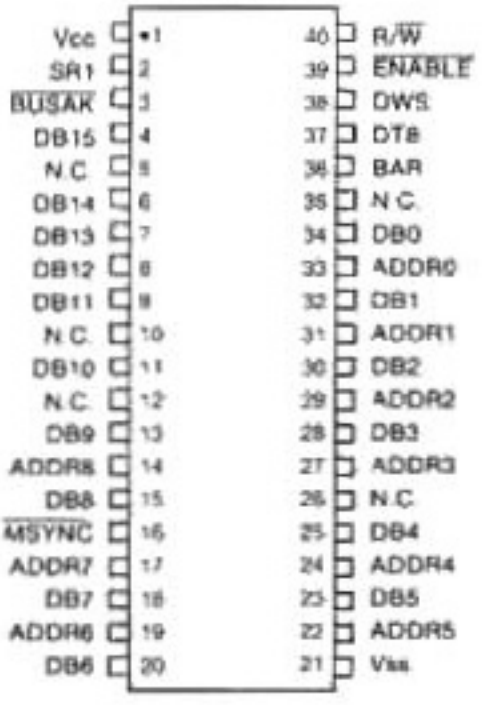
OPERATING DESCRIPTION

The device operates in three memory configurations. These configurations are selected via the input control signals.

1. When SR1 has been pulsed negative, the memory is located at 12288 to 14335. The external memory is addressed at 14336 to 16383.
2. When BUSAK has been pulsed negative, the memory is located at 0 to 2047. The external memory is addressed at 2048 to 4095.
3. When BAR and DWS are pulsed positive, the memory will not respond to address bit 9 and address bit 10, which restricts the memory to 512 locations. The memory is now located from 0 to 511 relative to the current memory origin. The external memory is also addressable from 0 to 511 relative to its current origin. Configuration three may be released by applying a negative pulse on the SR1 input.

Pin Configurations
40 Lead Dual In Line

Top View



*For more detailed data refer to General Instrument data specification book

TECHNICAL INFORMATION: AY-3-8900-1 (0098-640) U4

AY-3-8900-1*

STANDARD TELEVISION INTERFACE CHIP (STIC)

FEATURES

- Outputs include coded signal timings for NTSC compatible video signal generation
- Operation from a 3.579545MHz clock
- 8 coordinate addressable foreground objects on a grid of 167H by 105V of which 159 x 96 are visible positions
- Foreground objects independently programmable for half height, y zoom, x zoom and 8 or 16 character lines high
- Selectable background display on a matrix of 20H x 12V using 8 x 8 picture elements
- Capable of accepting data, address and graphics information on common multiplexed bus
- 16 digitally selectable colors

DESCRIPTION

The AY-3-8900-1 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900-1 operates within the computer system by time sharing a bidirectional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900-1 has switched to the CPU controlled mode. SR2 is issued thirteen or fourteen times per picture frame depending on picture offset. The AY-3-8900-1 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900-1 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also issued during the CPU controlled mode in response to BAR, ADAR or DW to enable an external device onto the 14 bit BUS.

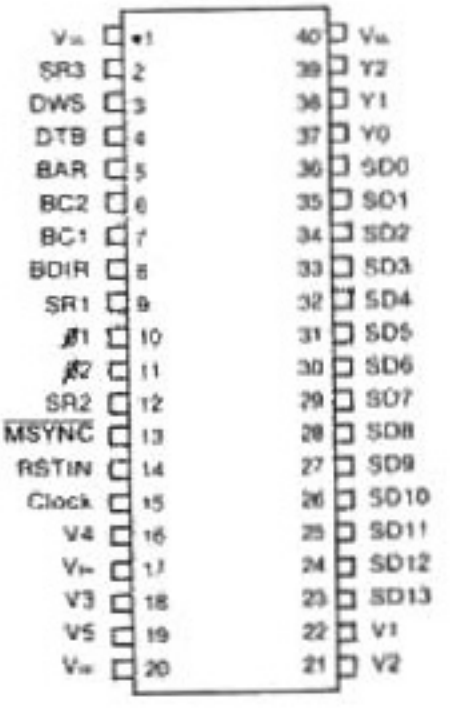
The second control bus is used to specify address, read and write sequences for the area of external memory used to store the graphic character "dot" patterns. The three signals on this BUS are BAR, DTB and DWS. The BAR is output by the AY-3-8900-1 when a valid graphics character address is on the 14 bit BUS. The external memory must latch this address for future read or write operations. The DTB signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit BUS. The DWS signal indicates that a "write" is requested.

The graphics control BUS is used during STIC time in the fetch of "foreground" object patterns and "background" object patterns. During the non STIC time when in the CPU controlled mode, the graphics control BUS can be used to link the memory area containing the graphics patterns to the main memory area of the external microprocessor.

The third control BUS communicates with the external CPU. This BUS comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control BUS is only validated if the AY-3-8900-1 is in the CPU controlled mode, otherwise it is ignored.

Pin Configurations
40 Lead Dual In Line

Top View



*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: AY-3-8914 (0098-0660) U6

AY-3-8914*

PROGRAMMABLE SOUND GENERATOR

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmed analog outputs
- Two 8-bit general purpose I/O ports
- Single +5 Volt Supply

DESCRIPTION

The AY-3-8914 Programmable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8914 is manufactured in GI's N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock and a microprocessor controller such as the GI 16-bit CP1600/1610 or one of GI's PIC 1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from subaudible at its lowest frequency to postaudible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8914 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package.

PIN FUNCTIONS

DA7—DA0 (input/output/high impedance) pins 30-37 (AY-3-8914)
Data/Address 7—0:

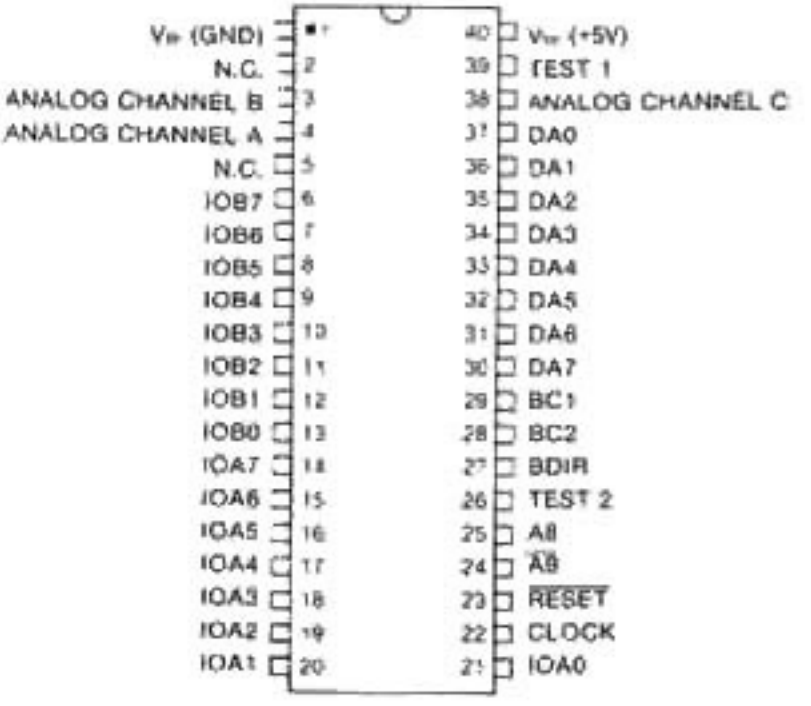
These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG in the data mode. DA-7—DA0 correspond to Register Array bits B-7—B0 in the address mode. DA3—DA0 select the register # (0—17s) and DA7—DA4 in conjunction with address inputs A9 and A8 form the high order address (chip select)

A8 (input) pin 25 (AY-3-8914)
$\overline{\text{A9}}$ (input) pin 24 (AY-3-8914)

Address 9. Address 8

These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1.024 word memory area rather than in a 256 word memory area as defined by address bits DA7—DA0 alone. If the memory size does not require the use of these extra address lines, they may be left unconnected as each is provided with either an on-chip pull down (A9) or pull-up (A8) resistor in "noisy"environments, however, it is recommended that A9 and A8 be tied to an external ground and +5V respectively if they are not to be used.

Pin Configurations
40 Lead Dual In Line
Top View



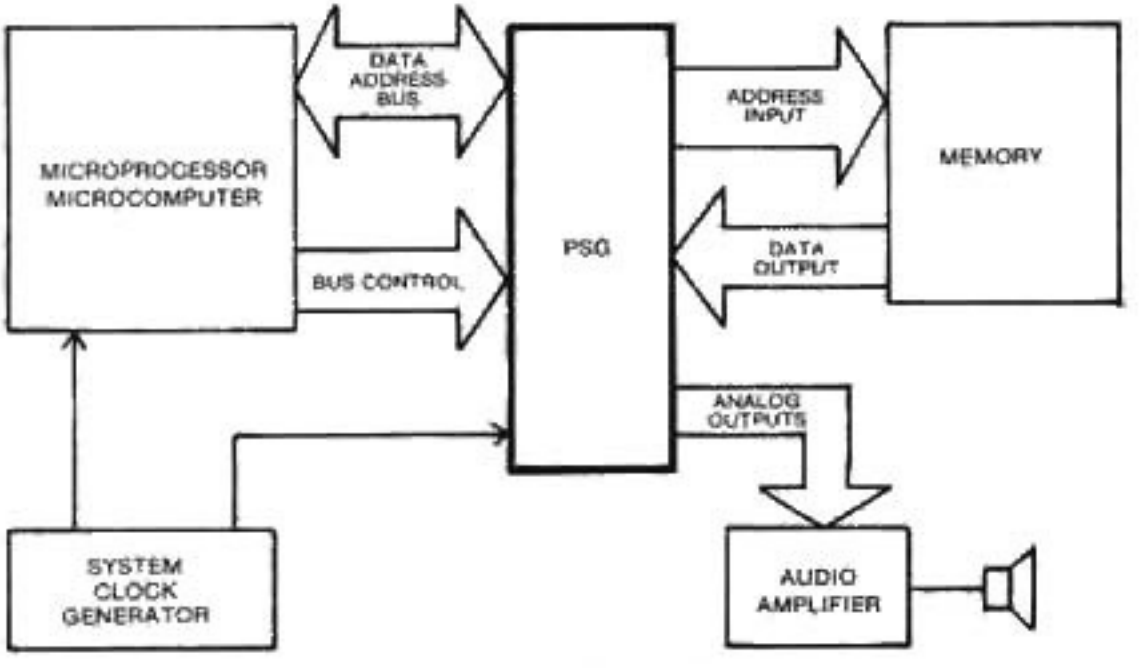


Fig. 1 SYSTEM BLOCK DIAGRAM

*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: RO-3-9502 (0098-0620) U9
RO-3-9502*

SYSTEM ROM

FEATURES

- Mask programmable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Control decoder
- Programmable memory map circuitry to place 2K ROM page within 65K word memory space located on 2K page boundaries
- Master logic with programmable 16 bit vectored start address
- Interrupt logic with programmable 16 bit vectored interrupt address
- 16 bit static address outputs for external memory
- Control signals for external memory:
  ENABLE = (DTB) • DWS) Address External = $R/\overline{E}$
  WRITE = DWS. Address External = $R/\overline{W}$
- Programmable memory map selection for external memory area
- Bus drive capability, 1 TTL load and 100pF plus tri-state

CIRCUIT REQUIREMENTS

The RO-3-9502 operates as the system memory for systems using a CP1610 series microprocessor.

It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

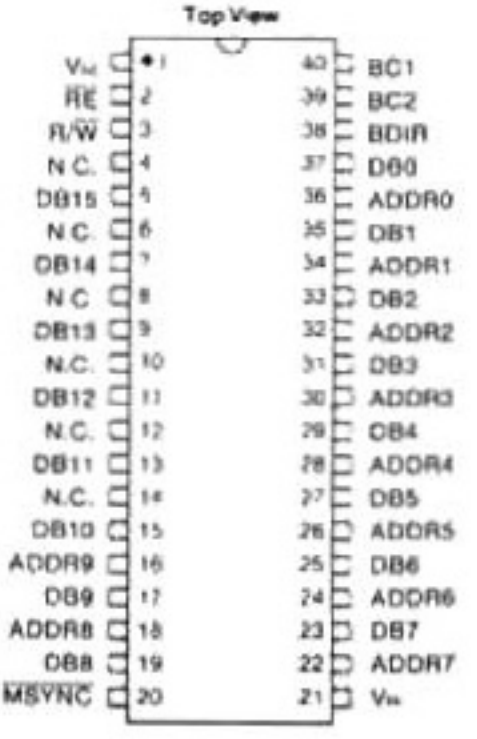
OPERATING DESCRIPTION

The RO-3-9502 is initialized by the MSYNC input and from the positive edge of this signal. It remains in a tri-state output condition, awaiting the IAB response. During the IAB the 9502 transmits a 16 bit code onto the external bus, thus providing the system start address vector. The completion of the MCLR sequence is recorded on chip such that any furthr IAB Codes output the second interrupt vector. From initialization, the 9502 waits for the first address code. For this address code and all subsequent address sequences, the 9502 reads the 16 bit external bus and latches the value into its address register. The contents of this address register are made available for connection to external memory and are supplied on 16 latched outputs with a drive capability of 1 TTL load and 100pF.

The 9502 contains a programmable memory map location for its own 2K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9502 will output the 10 bits of addressed data and also drive a logic zero on the top six bits of the bus.

*For more detailed data refer to General Instrument data specification book.

Pin Configurations
40 Lead Dual In Line



OPERATION WITH EXTERNAL MEMORY

The 16 bits from the address register are produced as static outputs for connection to external ROM or RAM devices. Two other signals are provided to control the external memory area. An enable signal is provided for any read or write operation, and a write signal for any move out operation. The two external memory control signals are gated by a min-max memory map comparator. The minimum and maximum values are programmable on boundaries within the 65K word memory area. The memory map comparator for external memory is a simple single compare and the operation is such that when a 2K area is chosen, a five bit compare is used and for a 4K area a four bit compare, etc. The effect of this is that 2K pages may start on 2K boundaries; i.e., 0, 2, 4, 6, 8, etc.; but 4K pages must be on 4K boundaries; i.e., 0, 4, 8, 12, etc. The same is true for 8K and 16K pages.

INPUT CONTROL SIGNALS

BDIR	BC1	BC2	Equivalent Signal	Response
0	0	0	NACT	NACT
0	0	1	IAB	IAB
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	
1	1	1	INTAK	—

*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: AY-3-8915 (0098-0680) U10

AY-3-8915*

COLOR PROCESSOR CHIP

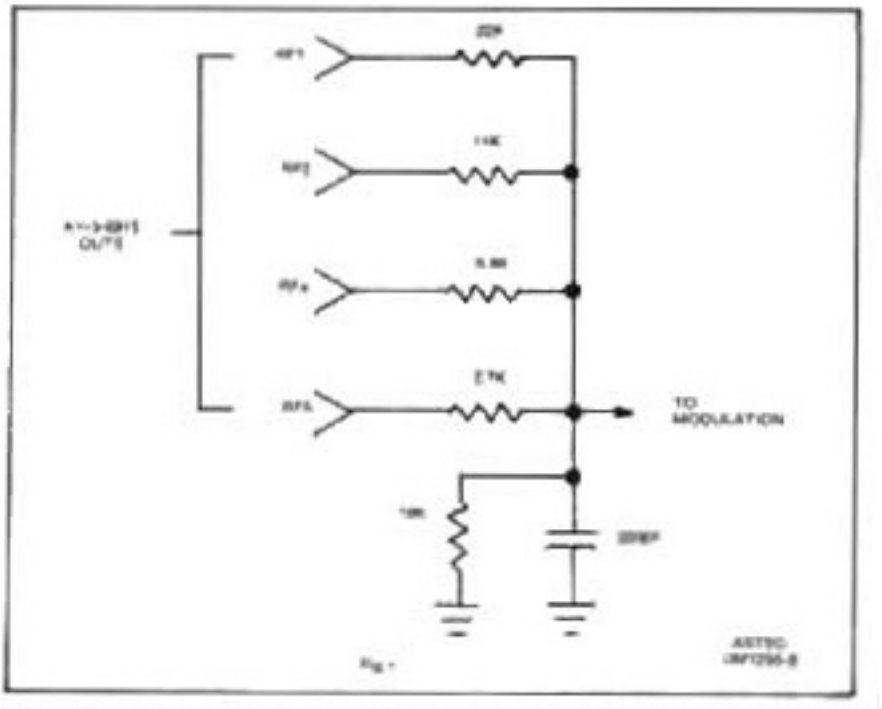
FEATURES

- Operation from 7.15909MHz crystal
- Five-line digital selection for 1 of 16 colors, blanking, sync and color burst
- 3.579545MHz buffered output

DESCRIPTION

The required color to be displayed for each 280 nsec PIXEL is decoded on a four line binary coded input. This selects one of sixteen possible colors. An external resistor network completes the D to A function as shown in the schematic Fig. 1 of this document. The waveform plus table illustrates the use of the five inputs to produce composite sync, color burst, line blanking, frame blanking and video

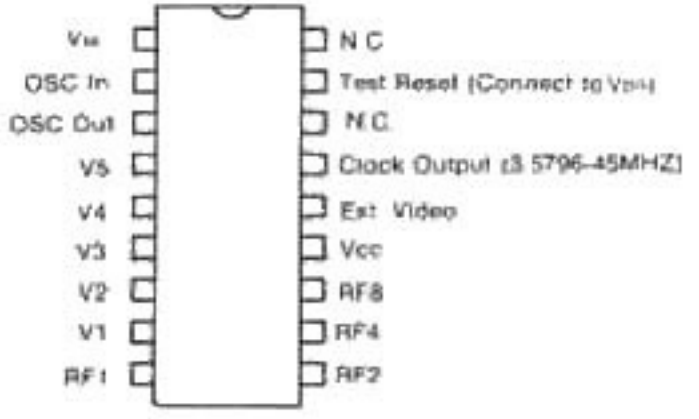
The external video input pin provides the ability to superimpose white high resolution (140 nsec wide) video information over the picture (color image).

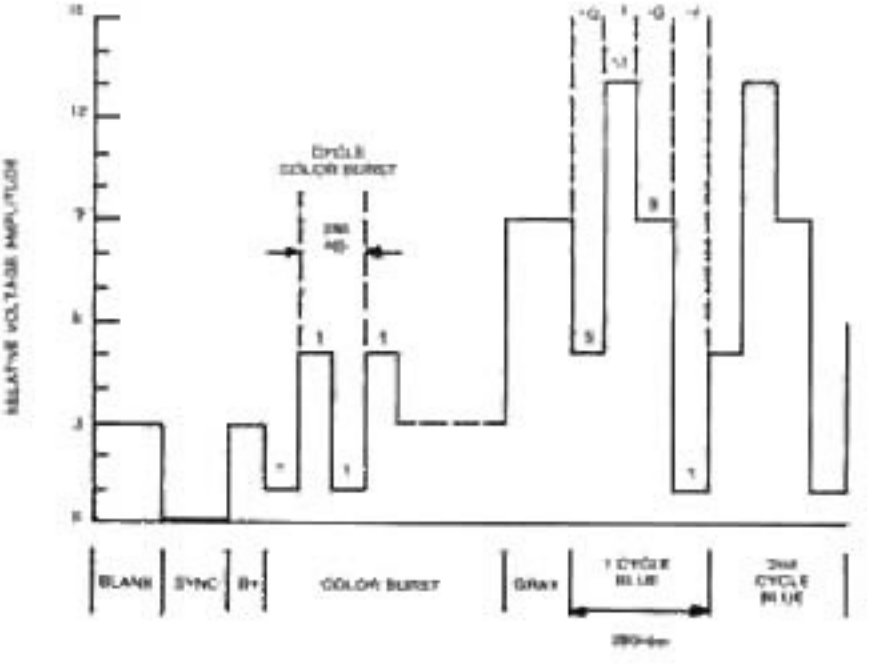


INPUT CODE ASSIGNMENT					TIME SLOT RELATIVE VOLTAGE AMPLITUDES				COLOR OUTPUT DESCRIPTION	
V5	V4	V3	V2	V1	+Q	- I	- Q	+I		
0	0	0	0	0	3	3	3	3	Black	
0	0	0	0	1	5	13	9	1	Blue	
0	0	0	1	0	3	0	4	12	Red	
0	0	0	1	1	4	4	12	12	Tan	
0	0	1	0	0	3	8	11	6	Grass Green	Group A
0	0	1	0	1	3	11	13	5	Green	
0	0	1	1	0	9	11	15	13	Yellow	
0	0	1	1	1	13	13	13	13	White	
0	1	0	0	0	9	9	9	9	Grey	
0	1	0	0	1	8	13	12	7	Cyan	
0	1	0	1	0	9	4	9	14	Orange	
0	1	0	1	1	4	4	8	8	Brown	
0	1	1	0	0	13	5	3	11	Magenta	Group B
0	1	1	0	1	12	12	6	6	Light Blue	
0	1	1	1	0	5	9	13	9	Yellow-Green	
0	1	1	1	1	10	5	2	7	Purple	
1	x	x	0	0	3	3	3	3	Blanking	
1	x	x	1	0	1	1	5	5	Color Burst	
1	x	x	0	1	0	0	0	0	Sync	
1	1	1	1	1	0	15	0	15	Test	

x = Don't Care

PIN CONFIGURATIONS
18 LEAD DUAL IN LINE





*For more detailed data refer to General Instrument data specification book.

TECHNICAL INFORMATION: 3539 (0098-0690) U7 U8 U12

3539*

256 x 8 RAM (GRAPHICS RAM, SCRATCH PAD RAM)

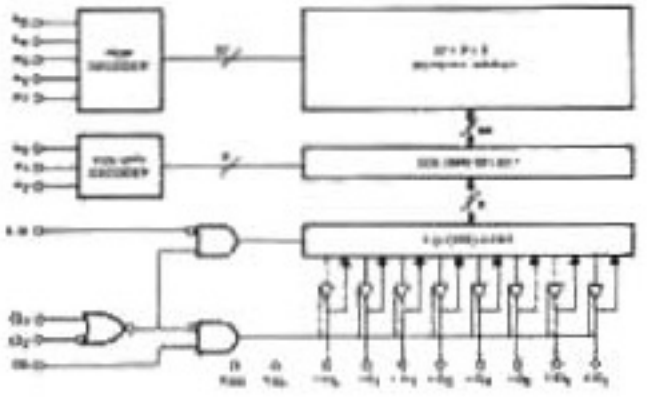
FEATURES

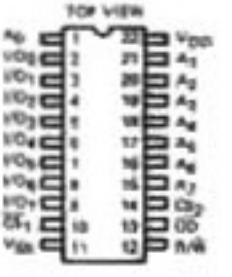
- 256 words x 8 bits
- 500 nSEC maximum access time
- Less than 400 mW power (Standard device)
- Less than 210 mW power (Low Power device)
- Single +5V power supply
- Two separate Chip Select inputs
- Separate Output Disable function
- Ideal replacement for 2111 and 2112 RAMs
- Fully compatible with all GTE byte-wide RAMs

GENERAL DESCRIPTION

The GTE 3539 Static RAM is a 2048-bit (256 x 8) memory device with a maximum access time of 400 nanoseconds. The 3539 is ideally suited for byte-oriented small memory applications and as a functional replacement for 2111 and 2112 Static RAMs. Complimentary Chip Select (CS and $\overline{CS}$) inputs are provided in addition to a separate Output Disable ($\overline{OD}$) function which allows gating output data onto the I/O bus on command. An 8-bit common I/O bus allows convenient interfacing to byte-wide design applications. The 3539 is available in 400 and 500 nanoseconds access times, and a choice of Standard (400 mW max.) or Low Power (210 mW max.) configurations. The 3539 is available in a standard 22-pin plastic or cerdip package.

Block Diagram





Pin Configuration and Logic Symbol

A_n	Address Inputs
CS_n	Chip Select Inputs
$\overline{OD}$	Output Disable
$R/\overline{W}$	Read/Write Control Input
I/O_n	Data Bus Pins
V_{DD}	+5 V Power Supply
V_{SS}	0 V Power Supply

TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OD}$	$R/\overline{W}$	STATUS	I/O BUS MODE
H	X	X	X	DESELECTED	HI Z
X	L	X	X	DESELECTED	HI Z
L	H	L	L	WRITE MODE	OUTPUT DISABLED DATA CAN BE WRITTEN
L	H	H	L	WRITE MODE	OUTPUT ENABLED DATA CANNOT BE WRITTEN
L	H	L	H	READ MODE	OUTPUT DISABLED DATA CANNOT BE READ
L	H	H	H	READ MODE	OUTPUT ENABLED DATA CAN BE READ

x = Don't Care

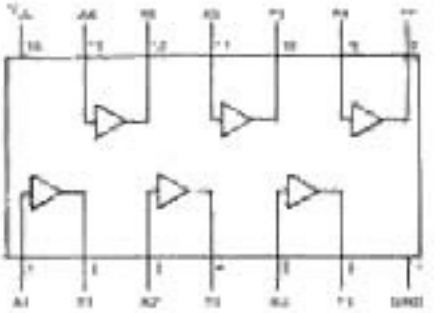
*For more detailed data refer to GTE technical specifications book.

TECHNICAL INFORMATION: HD7407P (0098-2110) U11

HEX BUFFER WITH OPEN-COLLECTOR HIGH VOLTAGE OUTPUTS

TRUTH TABLE

INPUT	OUTPUT
A	Q
L	L
H	H

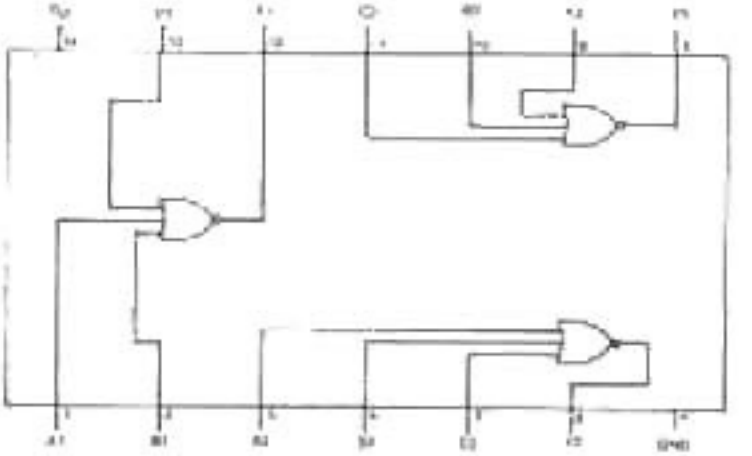


HD74LS27P (0098-2600) U13

TRIPLE 3-INPUT NOR GATES

TRUTH TABLE

INPUT			OUTPUT
A	B	C	Q
L	L	L	H
H	L	L	L
L	H	L	L
L	L	H	L
H	H	L	L
L	H	H	L
H	L	H	L
H	H	H	L

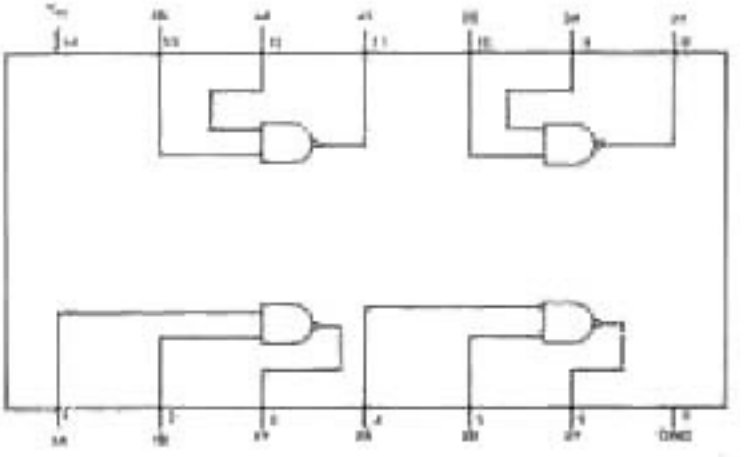


HD74LS00P (0098-2520) U16

QUAD 2-INPUT NAND GATES

TRUTH TABLE

INPUT		OUTPUT
A	B	Q
L	L	H
H	L	H
L	H	H
H	H	L



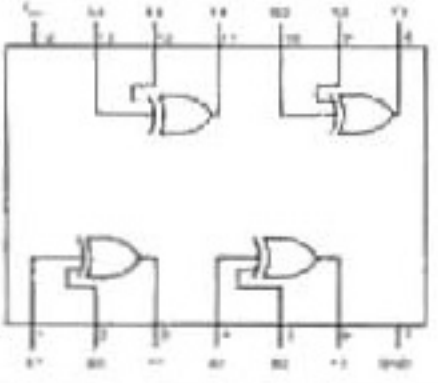
ELECTRICAL CHARACTERISTICS*

PARAMETER		CONDITIONS	7407 (U11)	74LS27 (U13)	74LS00 (U16)	74LS86 (U17)
VCC	SUPPLY VOLTAGE		5	5	5	5
TA	TEMP. AMBIENT		25	25	25	25
VIH	HIGH LEVEL INPUT		MIN 2	MIN 2	MIN 2	MIN 2
VIL	LOW LEVEL INPUT		MAX 0.8	MAX 0.8	MAX 0.8	MAX 0.8
VOH	HIGH LEVEL OUTPUT IOH = MAX	Vcc = MIN VIL = MAX VIH = 2V	MIN 2.4 TYP 3.4	MIN 2.4 TYP 3.4	MIN 2.4 TYP 3.4	MIN 2.4 TYP 3.4
VOL	LOW LEVEL OUTPUT IOL = MAX		MAX 0.4 TYP 0.2	MAX 0.4 TYP 0.2	MAX 0.4 TYP 0.2	MAX 0.4 TYP 0.2

QUAD 2-INPUT EXCLUSIVE -OR GATES

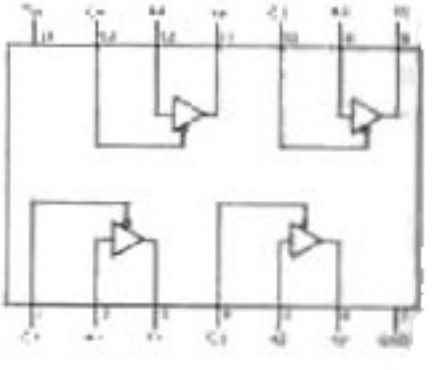
TRUTH TABLE

INPUT		OUTPUT
A	B	Q
L	L	L
H	L	L
L	H	H
H	H	L



HD74LS125AP (0098-2120) U14 & U15

TRI-STATE QUAD BUFFERS



ELECTRICAL CHARACTERISTICS:*

PARAMETER		CONDITIONS	74LS115	UNITS
VCC	SUPPLY VOLTAGE		5	V
TA	TEMP. AMBIENT		25	$^{O}_{C}$
VIH	HIGH LEVEL INPUT		MIN 2	V
VIL	LOW LEVEL INPUT		MAX 0.8	V
VOH	HIGH LEVEL OUTPUT	VCC = MIN	MIN 2.4	V
		VIL = MAX	TYP 3.1	
VOL	LOW LEVEL OUTPUT	VIH = 2V IOH = MAX	MAX 0.5 (IOL = MAX)	V

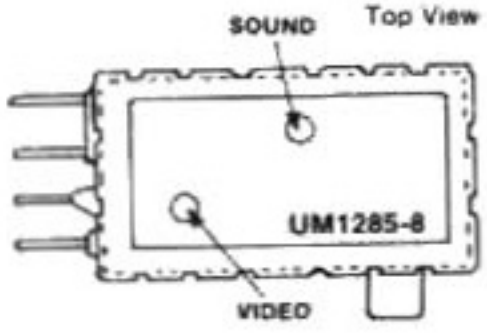
TRUTH TABLE

INPUTS		OUTPUTS
A	C	Y
H	L	H
L	L	L
X	H	HI-Z

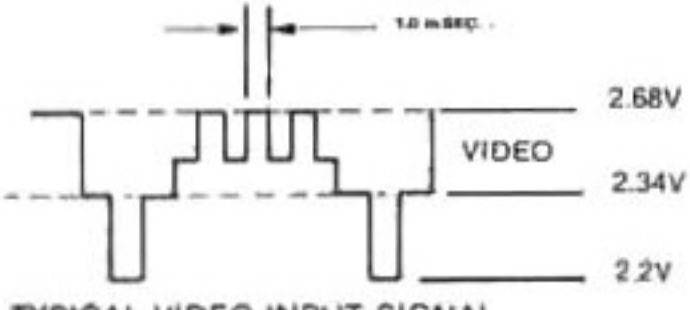
*For more detailed information consult IC data book

TECHNICAL INFORMATION: RF MODULATOR (2609-4689)

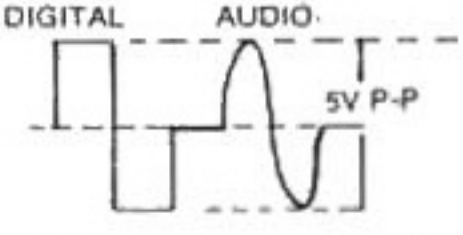
LEAD	IDENTIFICATION
(1)	VIDEO INPUT
(2)	VCC
(3)	AUDIO INPUT
(4)	CHANNEL SELECT (OVDC SELECTS CH3, OPEN SELECTS CH4)
(5)	RF OUTPUT



RF Modulator
(2609-4689)



TYPICAL VIDEO INPUT SIGNAL



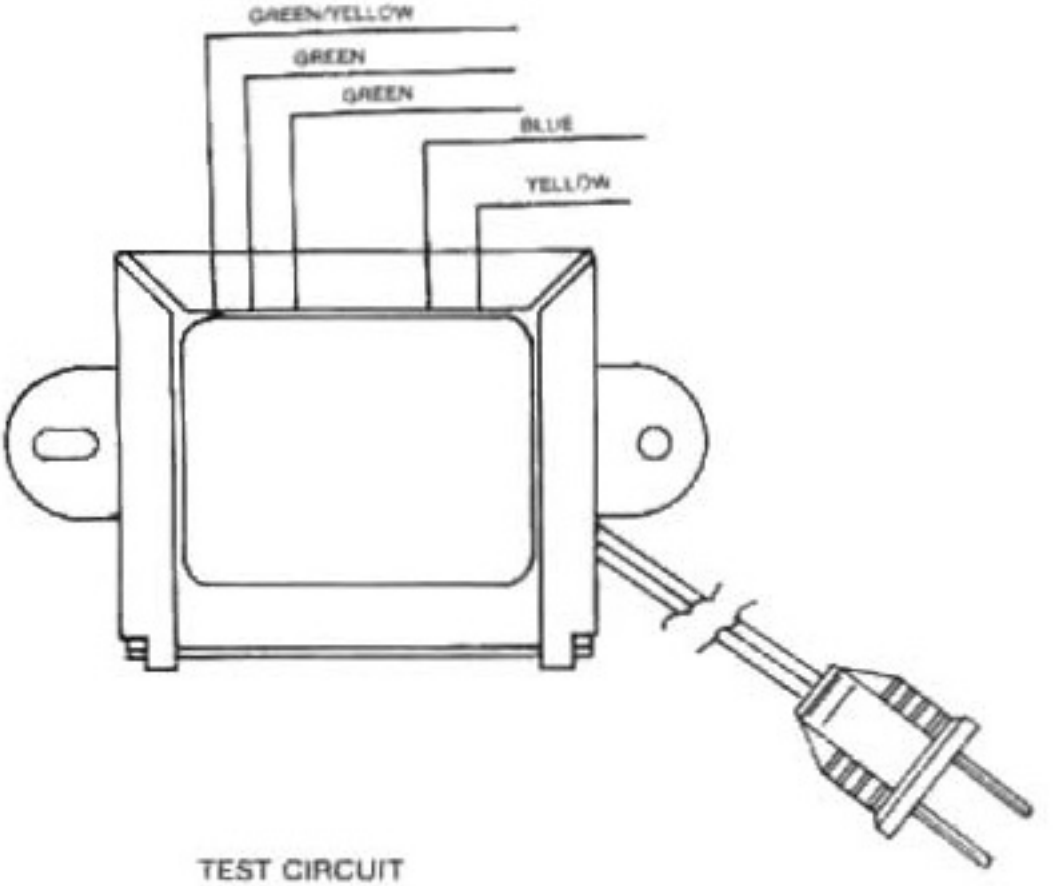
TYPICAL AUDIO INPUT SIGNAL

ELECTRICAL CHARACTERISTICS

Conditions of measurement – Vcc : +6V ±0.2V Ta : 25℃
Output terminated with 1.5M 75 ohm coax and 75 ohm load

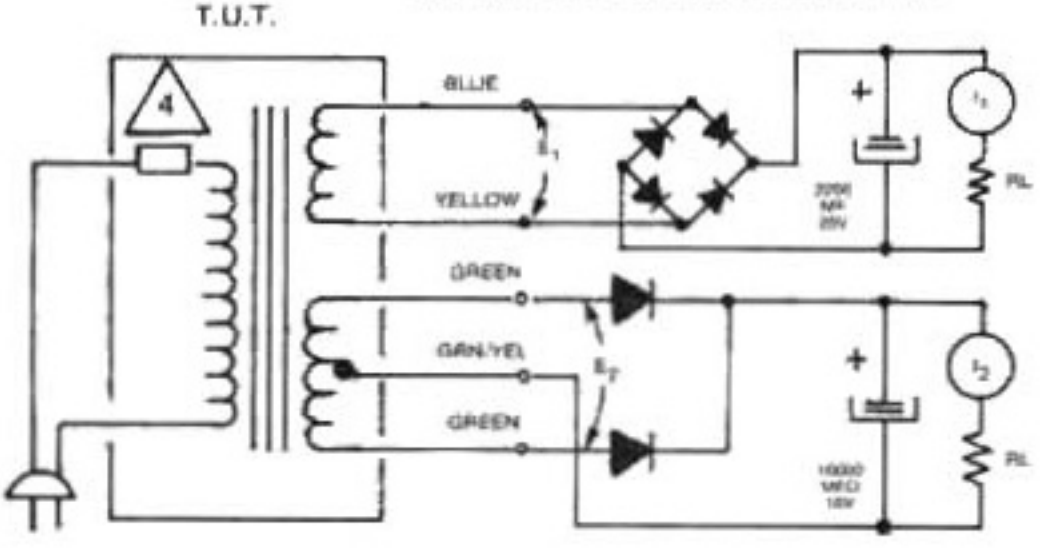
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Fc 3	Channel 3 Video Carrier @ 25℃	61.00	61.25	61.50	MHz
Fc 4	Channel 4 Video Carrier @ 25℃	67.40	67.65	67.90	MHz
Fsc	Sound Carrier @ 25℃	4.480	4.500	4.520	MHz
Vo (HI)	Video Carrier Output (Vmod = 2.2V)	0.8	1.5	2.5	mVrms
Vo (LO)	Video Carrier Output (Vmod = 2.8V)	14	18		-dB w.r.t. Vo (HI)
Vsco	Sound Carrier Output	26		18	-dB w.r.t. Vo (HI)
Vsp	Spurious/Harmonic			30	-dB w.r.t. Vo (HI)
ΔFc (T)	F for change in temp.			±10	KHz/℃
ΔFsc (T)	F for change in temp.			±750	Hz/℃
ΔFc (V)	F for 1 Volt change in Vcc			±30	KHz/V
ΔFsc (V)	F for 1 Volt change in Vcc			±5	KHz/V
Zo	RP Output Impedance		75		ohm
RF BW	-3dB Band width (RF) CH3	10	14		MHz
	CH4	4.5	5.0		MHz
ICC	Supply Current		30	40	mA
ΔF/V	F M Sensitivity	4.0	8	12	KHz/Volt
920 KHz	Chroma/Sound Beat Level	48	55		-dB w.r.t.
VSWR	Voltage Standing Wave Ratio (CH 3 & 4)		1.7	2.5	Vo (HI)
Vcc	Supply Voltage	12V±5% (thru 180 ohm ¼ watt resistor)			

TECHNICAL INFORMATION:
POWER TRANSFORMER (2609-9549)



TEST CIRCUIT

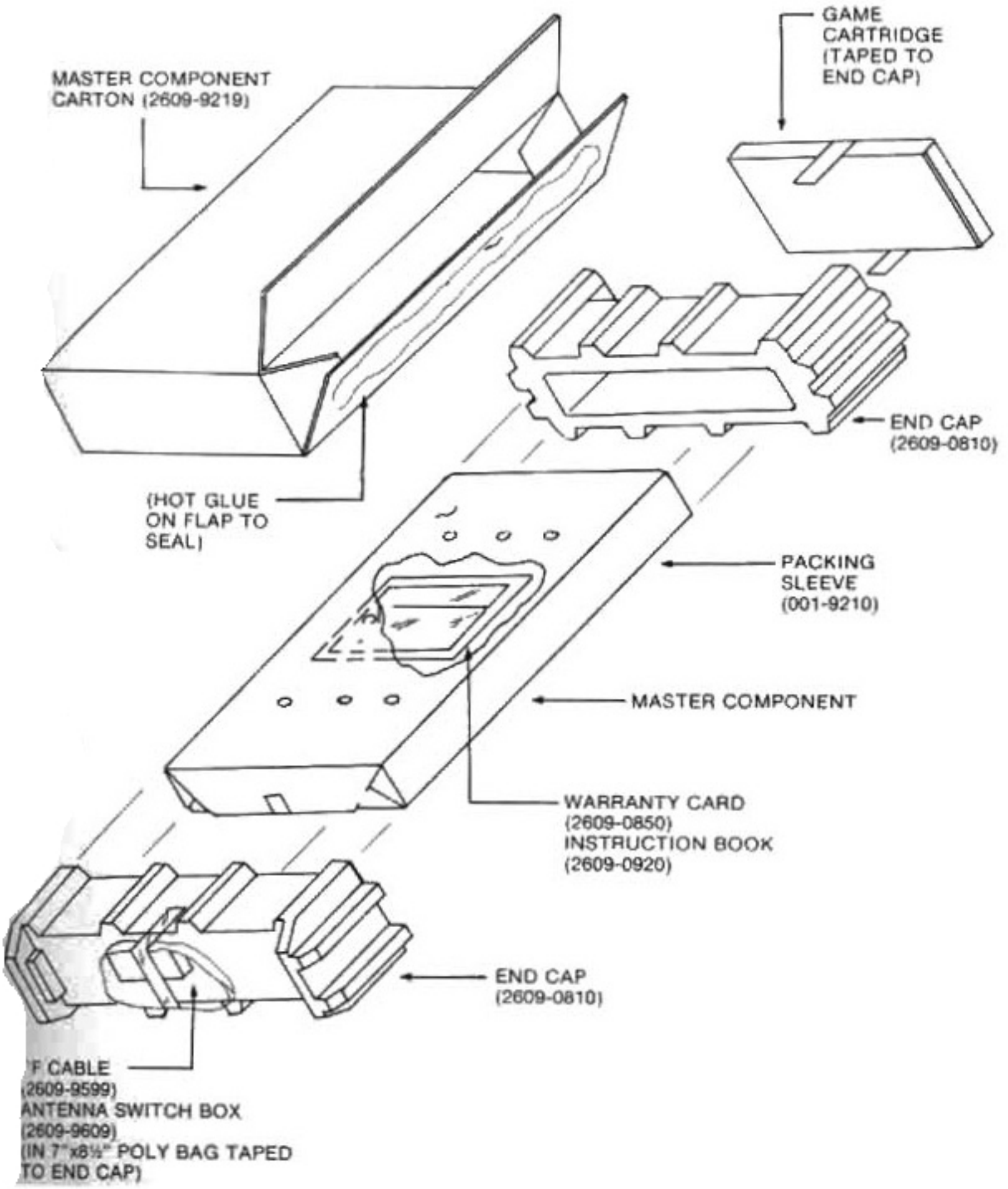
ALL DIODES ARE IN 4001 OR EQUIV.



PRIMARY
INPUT
115V AC
60 Hz

SECONDARY VOLTAGES
E_1 = 16.5 ±3% V AC @ I_1 = .275A DC
E_2 = 16.0 ±3% V AC @ I_2 = 1.0A DC

SECTION 8
PACKING INSTRUCTIONS



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