SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

purple binder, tab 6

SAA5070

MICROCOMPUTER/MICROPROCESSOR PERIPHERAL

IC FOR VIEWDATA (LUCY)

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface.
- Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parit
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters.
- Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

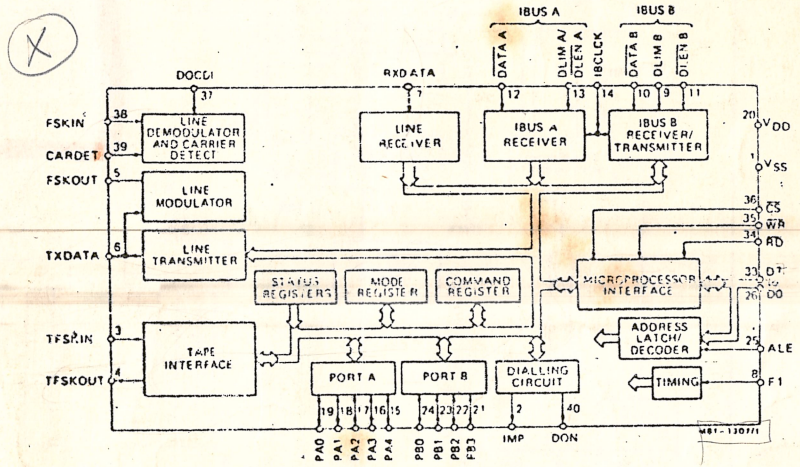
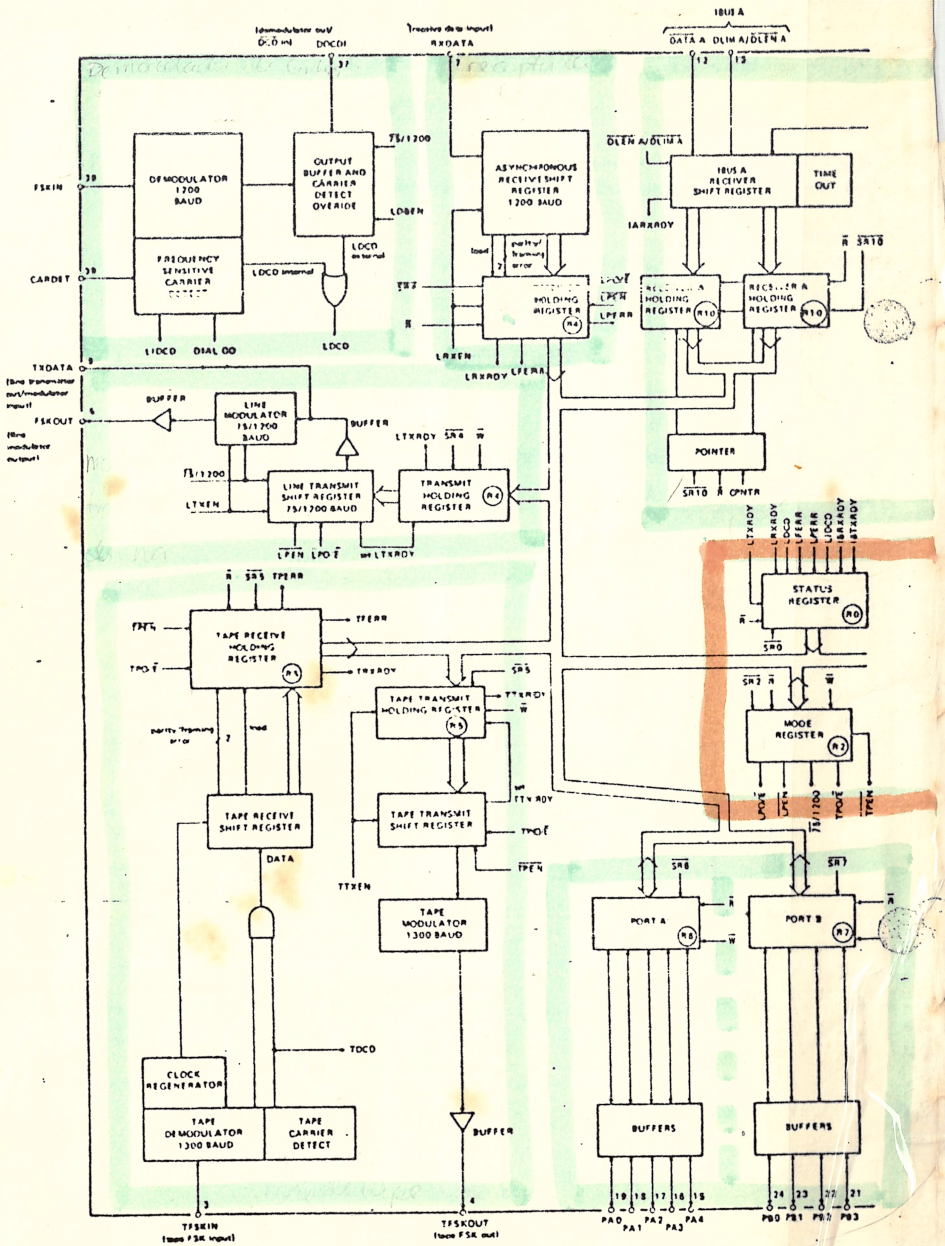


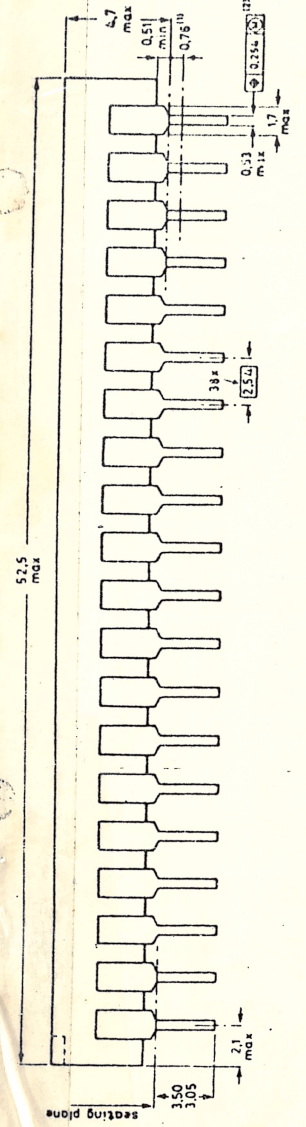
Fig.1a Simplified block diagram

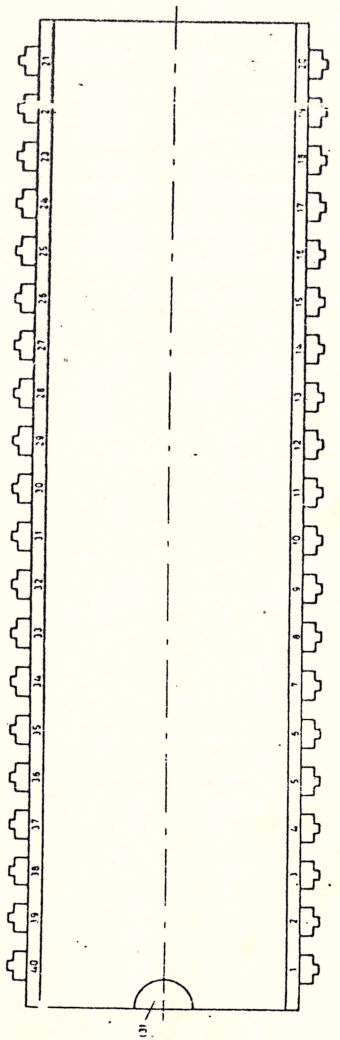
PACKAGE OUTLINE

40-lead DIL; plastic (SOT–129).



40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





Positional accuracy.

Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

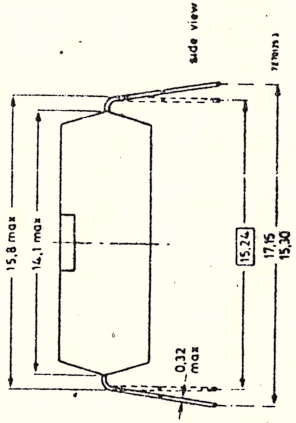
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page



MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready — data available
IBRXRDY	IBUS B receiver ready — data available
IBTXRDY	IBUS B transmitter ready — previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error — received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready — data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready — transmit holding register empty
$\overline{\text{SR}}$n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error — received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready — data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready — transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register

DEVELOPMENT SAMPLE DATA

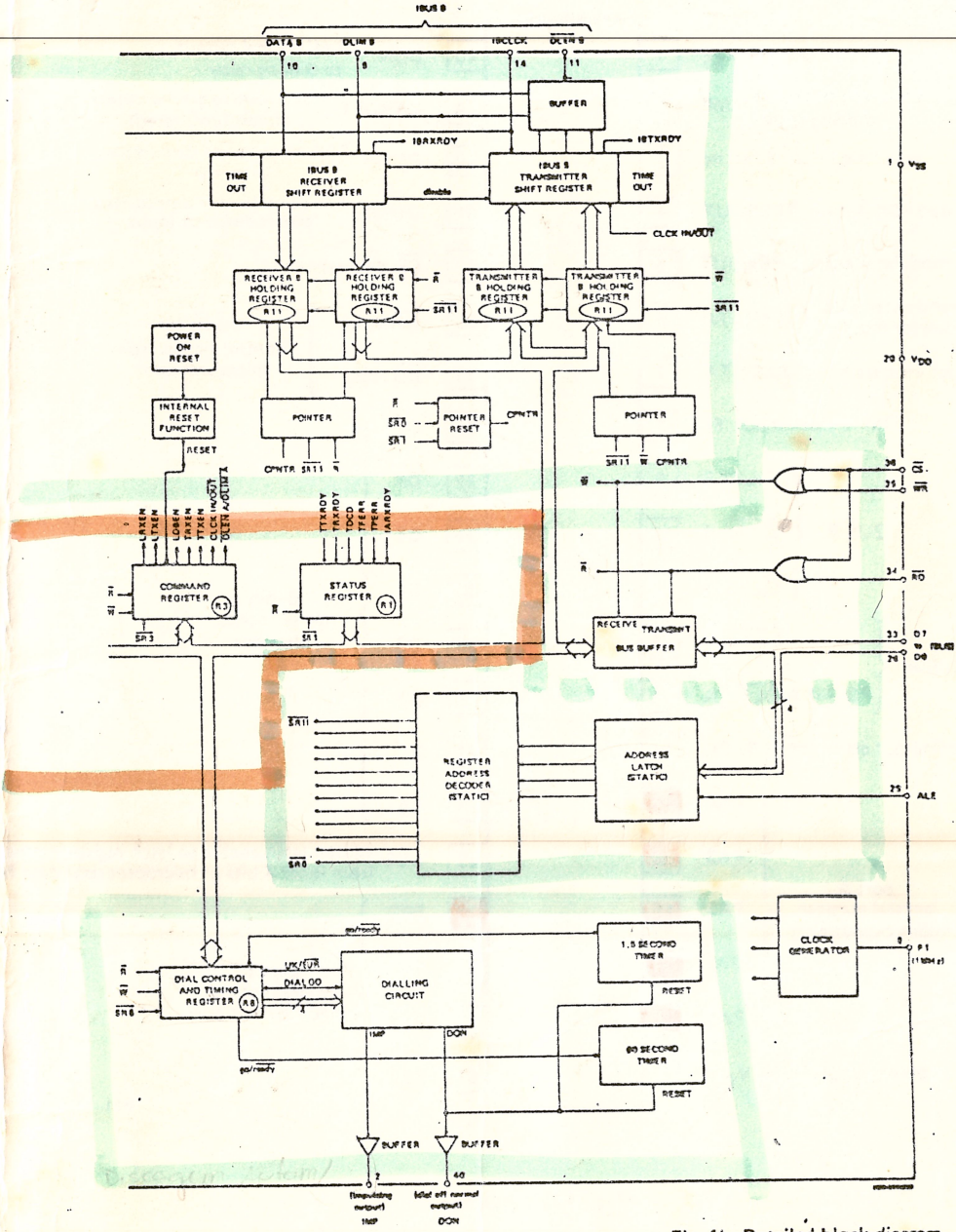


Fig. 1b. Detailed block diagram

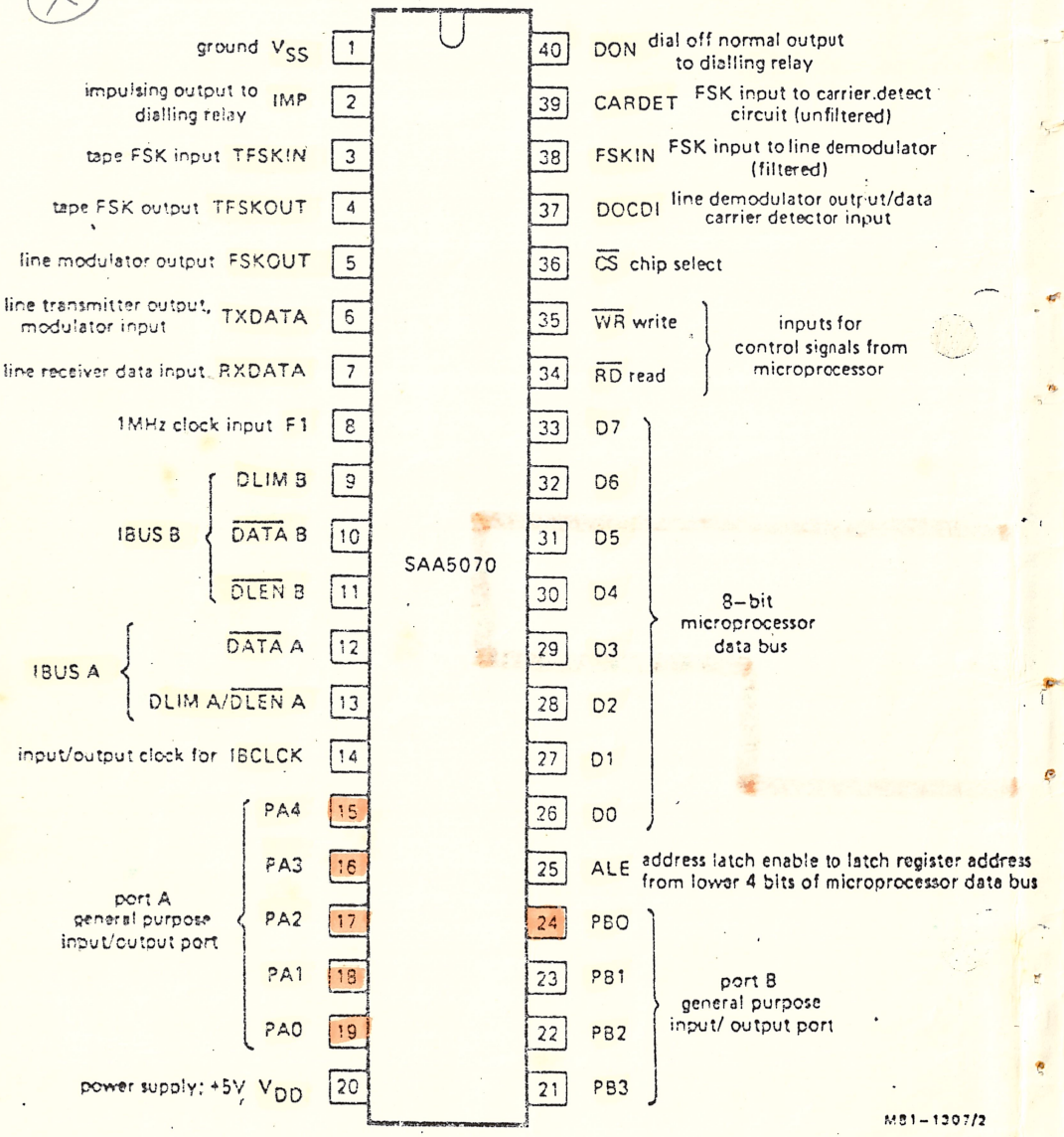


Fig.2 Pinning diagram

DEVELOPMENT SAMPLE DATA

APPENDIX

Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
	–	–	–	–	–	–	–	–	
R11 B	WL3 R/W	WL2 R/W	WL1 R/W	WL0 R/W	B12 R/W	B11 R/W	B10 R/W	B9 R/W	

NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LOCD R	LFERR R	LPERR R	LIOCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TOCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{LPEN}$ R/W	75/$\overline{1200}$ R/W		TPO/$\overline{E}$ R/W	$\overline{TPEN}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LOBEN R/W	TRXEN R/W	TTXEN R/W	CLK IN/$\overline{OUT}$ R/W	$\overline{DLEN}$ A/$\overline{DLIM}$ A R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R)	B7 R	B6 R	B6 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W)	B7 W	B6 W	B6 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{EUR}$ R/W	60s TIMER R/W	DIAL GO R/W	1.6s TIMER R/W	DI3 W	DI2 W	DI1 W	DI0 W	DIAL CONTROL AND TIMING REGISTER
R10A	B8 R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	IBUS A REGISTERS
R10B	WL3 R	WL2 R	WL1 R	WL0 R	B12 R	B11 R	B10 R	B9 R	

Mullard

DEVELOPMENT SAMPLE DATA

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all the operating frequencies. It performs most of the hardware functions of a viewdata terminal including an autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud modulator and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of pages of text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on separate ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynchronous transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an interface to a non volatile RAM which can store telephone numbers for autodialling and user passwords and Port B could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if required, in conjunction with the internal asynchronous receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter. Also the tape interface can work independently of, and simultaneously with, the line receiver.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5	V
Input voltage:					
PORT A (pins 15 to 19) and PB0 (pin 24)	V_I	−0.3	–	14.0	V
Input voltage (all other pins)	V_I	−0.3	–	7.5	V
Temperatures					
Storage temperature range	T_{stg}			−20 to +125	°C
Operating ambient temperature range	T_{amb}			−20 to +70	°C

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150	mA
Inputs					
All inputs (except F1 clock)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	µA
Input capacitance	C_I	–	–	7	pF

Data specific to certain inputs

		min.	typ.	max.	
F1 (1 MHz) Clock					
Input voltage; LOW	V_{IL}	−0.3	–	0.6	V
Input voltage; HIGH	V_{IH}	2.2	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Mark/space ratio (measured at 1.5 V level)		40:60	–	60:40	
$\overline{DATA}$ A, DLIM A/$\overline{DLEN}$ A (IBUS A)					
Data set up time (Fig.14)	t_{DS}	3	–	–	μs
Data hold time (Fig.14)	t_{DH}	3	–	–	μs
DLIM clock; HIGH (Fig.14)	t_{CH}	4	–	–	μs
DLIM clock; LOW (Fig.14)	t_{CL}	4	–	62	μs
Time between commands	t_{BC}	140	–	∞	μs
DLIM frequency	f_{DLIM}	16	–	160	kHz
ALE (Address Latch Enable) (Figs. 3 and 4)					
Pulse width (HIGH)	t_{ALEH}	400	–	–	ns
Cycle time	T_{ALE}	–	2500	–	ns
$\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ (Figs. 3 and 4)					
Control pulse width	t_{WL}	–	700	–	ns
Address hold time	t_{LA}	80	–	–	ns
Address set-up time	t_{AL}	120	–	–	ns
Read cycle timings (Fig.3)					
ALE to read pulse delay time	t_{ALR}	80	–	–	ns
Read pulse (falling edge) to data bus delay time	t_{RD}	–	–	500	ns
Data hold time	t_{DR}	0	–	200	ns
Write cycle timings (Fig.4)					
ALE to write pulse delay time	t_{ALW}	80	–	–	ns
Address set-up time to $\overline{WR}$	t_{AW}	230	–	–	ns
Data set up time before $\overline{WR}$	t_{DW}	500	–	–	ns
Data hold time after $\overline{WR}$	t_{WD}	120	–	–	ns

DEVELOPMENT SAMPLE DATA

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4.

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

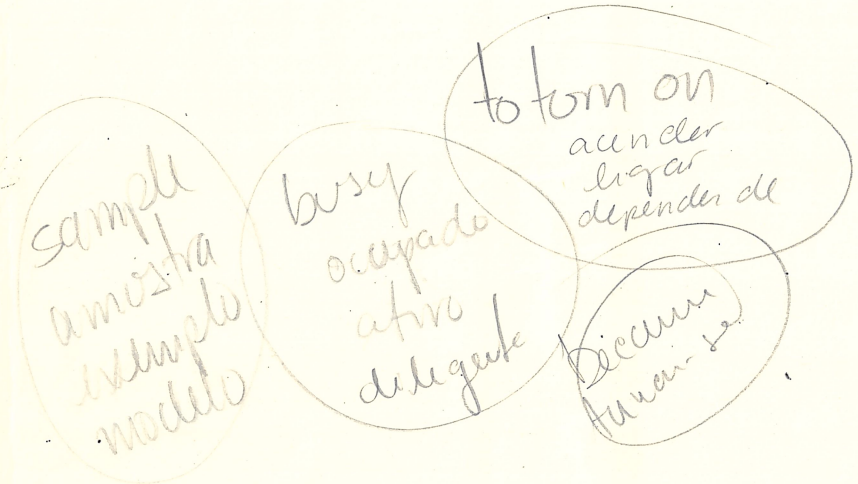
PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 5 V. PB0 is open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

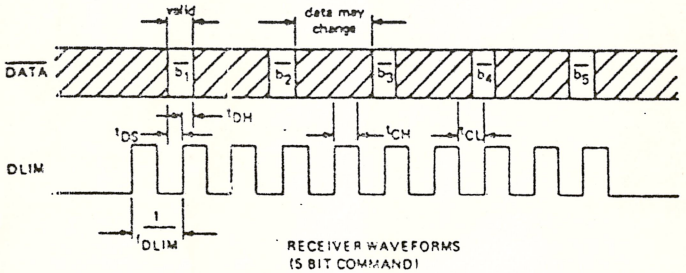


Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM).

Receiver B is inhibited from receiving data transmitted by transmitter B.

Receiver A may operated either as a two line receiver with $\overline{\text{DATA}}$ and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and $\overline{\text{CLK}}$ receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/DLIM A command D0, register R3 (command).

The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The functior is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3



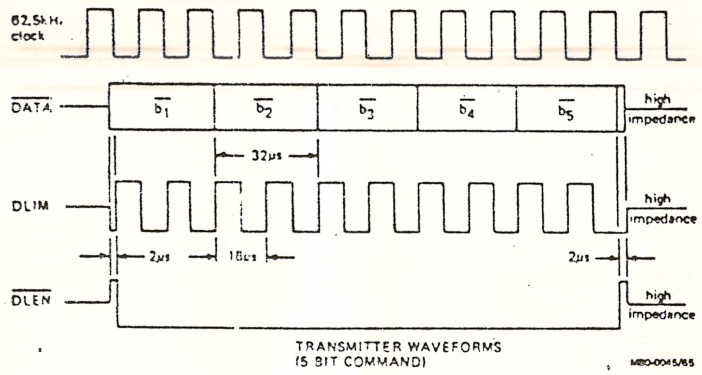


Fig. 14 IBUS waveforms

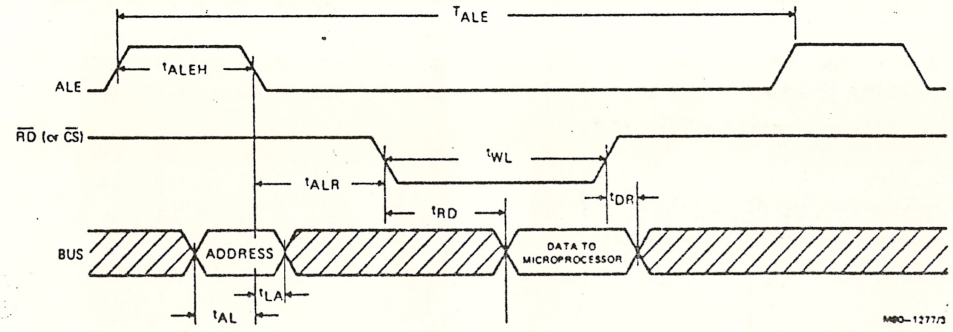


Fig.3 Read cycle timing

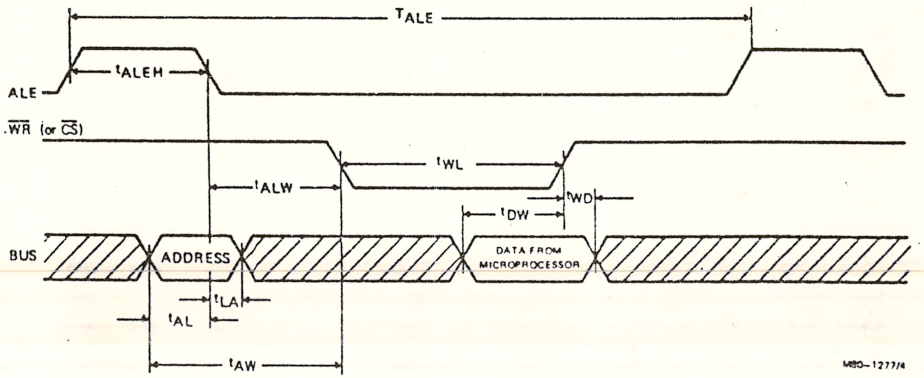


Fig.4 Write cycle timing

DEVELOPMENT SAMPLE DATA

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

$\overline{DATA}$ B, DLIM B, $\overline{DLEN}$ B, IBCLCK (IBUS B)			min.	typ.	max.	
Input voltage; LOW	Fig.14	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA),		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r | t_f	–	–	1	μs

other timings as IBUS A

DOCDI (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)		I_{IR}	–	0.4	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	0.4	–	V

TXDATA (Internal resistive pull-up, permitting wired - AND connection)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)		$-I_{IL}$	–	–	500	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)		V_{OH}	2.4	–	–	V
Load capacitance		C_L	–	–	40	pF
Output rise time (C_L = 40 pF)		t_r	–	3	–	μs

PA0 to PA4 (PORT A) (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	13.2	V
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)		I_{OR}	–	–	10	μA
Load capacitance		C_L	–	–	40	pF
Fall time		t_f	–	–	1	μs

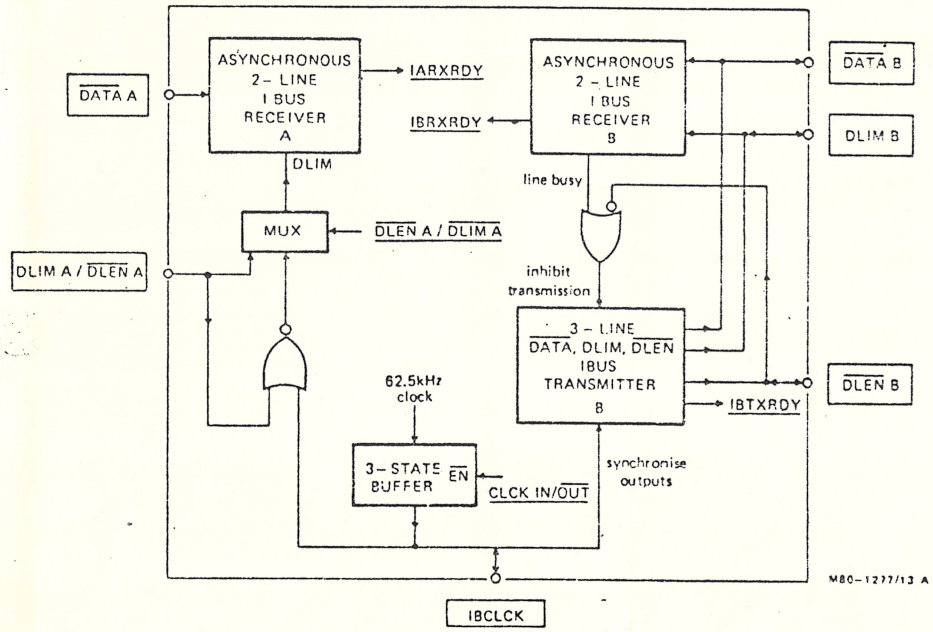


Fig.13 IBUS block diagram

For the transmitter the register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
TXB – R11A	8	7	6	5	4	3	2	1

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
XB – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

fashion = moda, estilo, modo

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes) – R10 – read only
Receiver B (2 bytes) – R11 – read only
Transmitter B (2 bytes) – R11 – write only

Associated flags in other registers:

IBRXRDY	–	D1	–	R0 (status)	– valid data available in receiver B holding register
IBTXRDY	–	D0	–	R0 (status)	– transmitter B holding register ready to accept new data
IARXRDY	–	D1	–	R1 (status)	– valid data available in receiver A holding register
CLCK IN/$\overline{OUT}$	–	D1	–	R3 (command)	– input/output control for 62.5 kHz pin
$\overline{DLEN}$ A/$\overline{DLIM}$ A	–	D0	–	R3 (command)	– 3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{DATA}$ A	– input	–	receiver A data input
DLIM A/$\overline{DLEN}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{DATA}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{DLEN}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

Inputs/Outputs (continued)		min.	typ.	max.	
PB0 (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	–0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	–0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r, t_f	–	–	150	ns

Outputs

These are protected against connection to V_{SS} or V_{DD}.

FSKOUT and TFSKOUT					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r, t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V

Autodialling timings are given in Fig.6

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.

An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 – I/O – 8-bit input/output port

Associated pins:

ALE	input	address latch enable from microprocessor
$\overline{WR}$	input	write pulse from microprocessor
$\overline{RD}$	input	read pulse from microprocessor
$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: – R8 – D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins:

DON	output	to drive dialling relays
IMP	output	

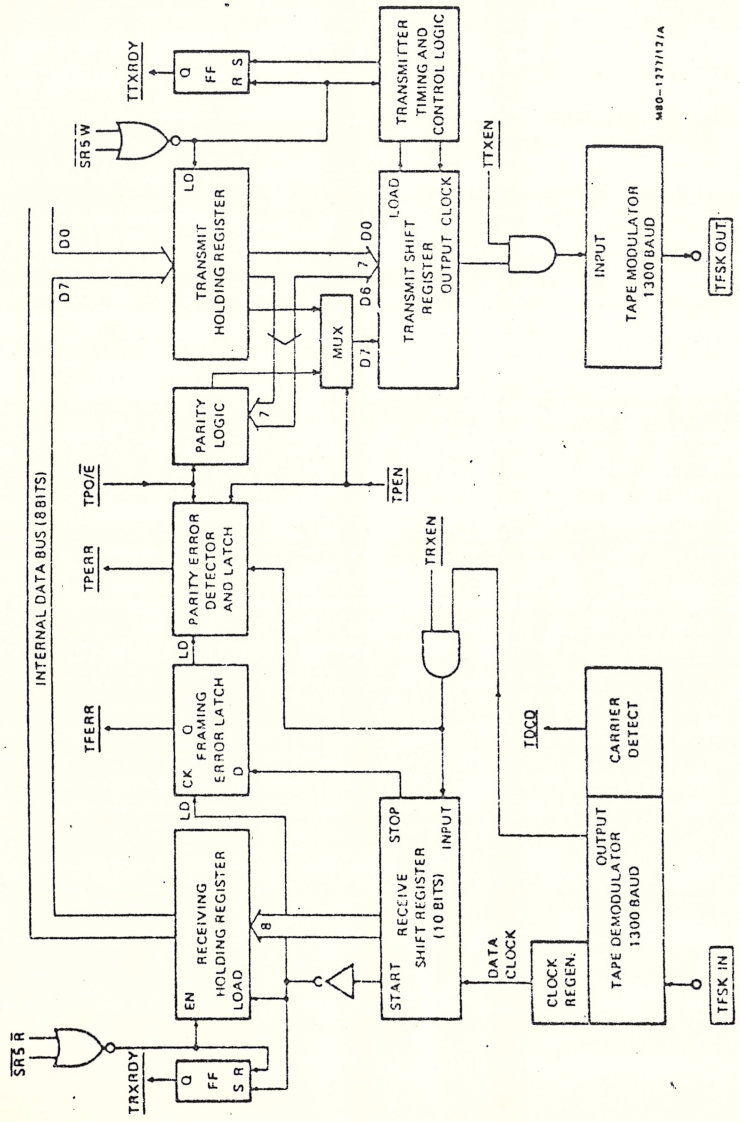


Fig.12 Tape section block diagram