This information is [illegible] made available for evaluation. It does not necessarily imply that the device will go into regular production.

purple binder, tab 6

MICROCOMPUTER/MICROPROCESSOR PERIPHERAL

IC FOR VIEWDATA (LUCY)

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface. • Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parit
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters. • Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

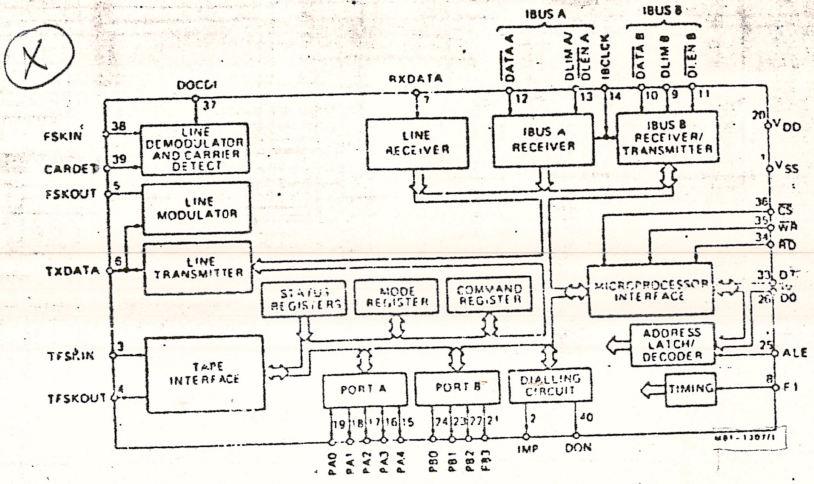

Fig.1a Simplified block diagram

PACKAGE OUTLINE

40 lead DIL; plastic (SOT–129).

Mullard

June 1981

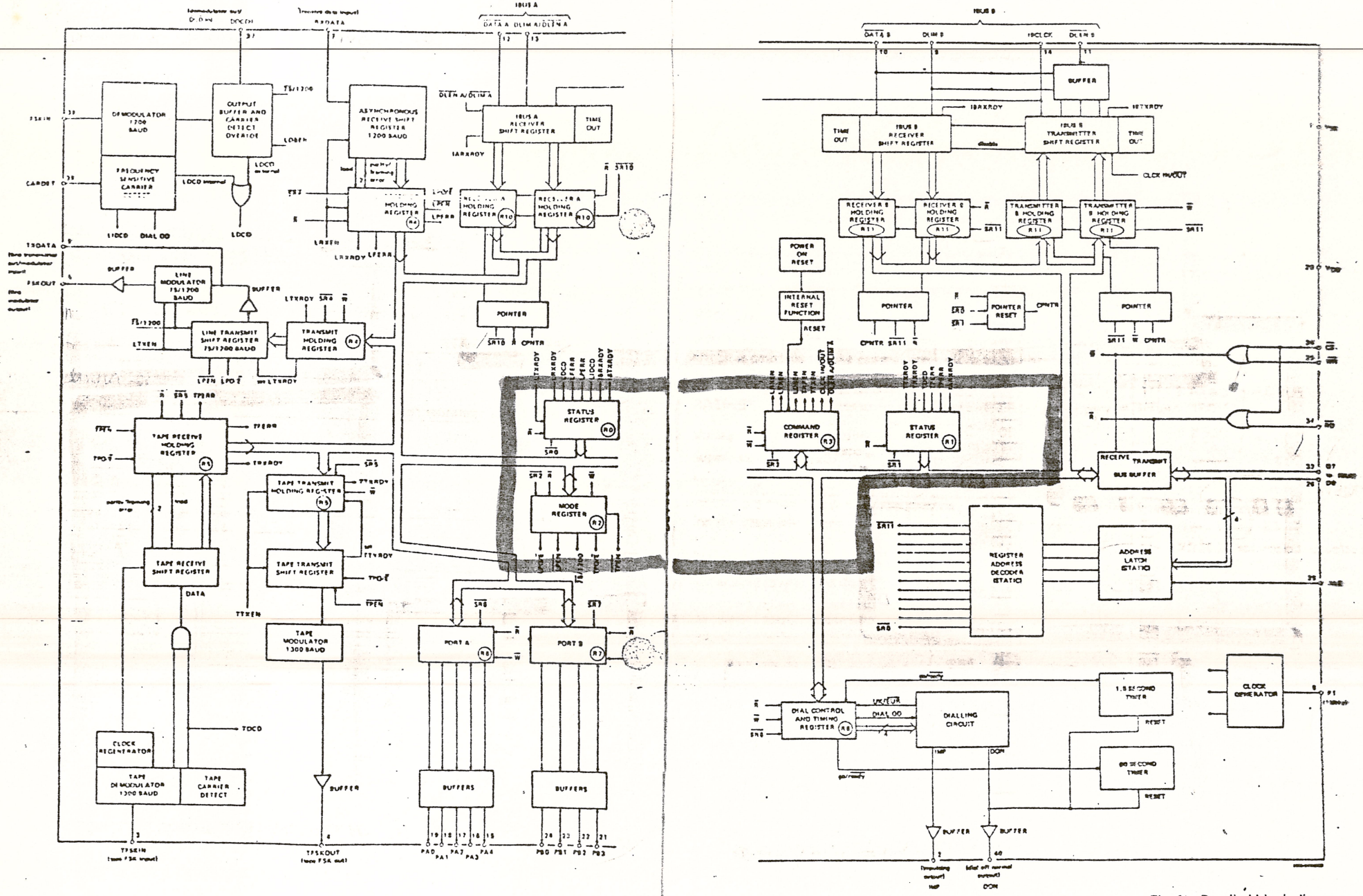

Fig. 1b. Detailed block diagram

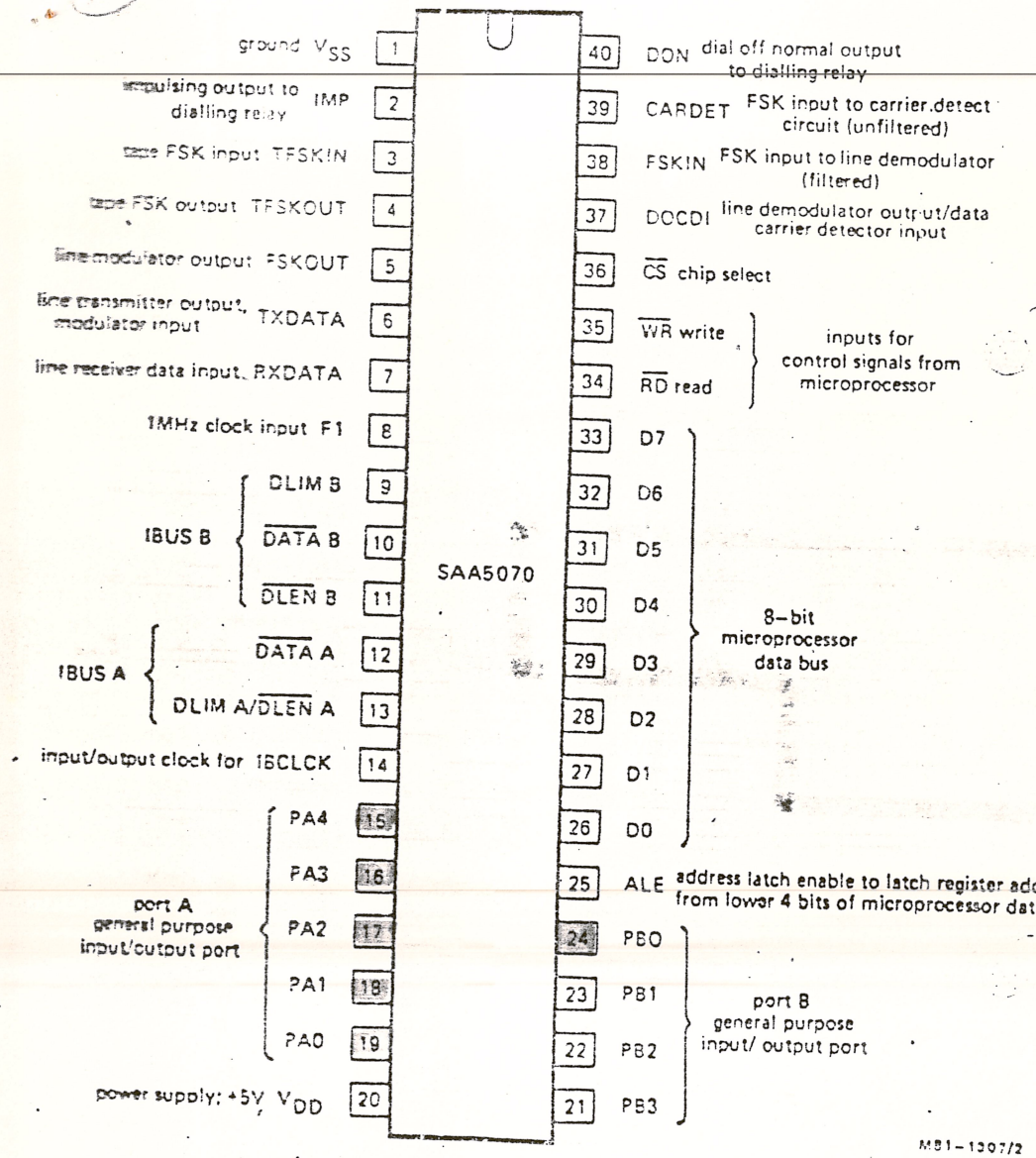

Fig.2 Pinning diagram

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all t operating frequencies. It performs most of the hardware functions of a viewdata terminal includ autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud m and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of p text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on sepa ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynch transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an i to a non volatile RAM which can store telephone numbers for autodialling and user passwords an could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if n conjunction with the internal asynchronous receiver and transmitter, or the internal modem ca independently of the internal receiver and transmitter. Also the tape interface can work indepenc and simultaneously with, the line receiver.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HAND MOS DEVICES').

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

		min.	typ.	max.
Voltages (with respect to pin 1)				
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5
Input voltage:				
PORT A (pins 15 to 19) and PB0 (pin 24)	V_I	−0.3	–	14.0
Input voltage (all other pins)	V_I	−0.3	–	7.5
Temperatures				
Storage temperature range	T_{stg}			−20 to +125
Operating ambient temperature range	T_{amb}			−20 to +70

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150
Inputs				
All inputs (except F1 clock)				
Input voltage; LOW	V_{IL}	−0.3	–	0.8
Input voltage; HIGH	V_{IH}	2.0	–	5.5
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10
Input capacitance	C_I	–	–	7

Data specific to certain inputs

	min.	typ.	max.	
E1 (1 MHz) Clock				
Input voltage; LOW	V_{IL}	−0.3	–	0.6 V
Input voltage; HIGH	V_{IH}	2.2	–	5.5 V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10 μA
Input capacitance	C_I	–	–	7 pF
Mark/space ratio (measured at 1.5 V level)		40:60	–	60:40
$\overline{DATA}$ A, DLIM A/$\overline{DLEN}$ A (IBUS A)				
Data set up time (Fig.14)	t_{DS}	3	–	– μs
Data hold time (Fig.14)	t_{DH}	3	–	– μs
DLIM clock; HIGH (Fig.14)	t_{CH}	4	–	– μs
DLIM clock; LOW (Fig.14)	t_{CL}	4	–	62 μs
Time between commands	t_{BC}	140	–	∞ μs
DLIM frequency	f_{DLIM}	16	–	160 kHz
ALE (Address Latch Enable) (Figs. 3 and 4)				
Pulse width (HIGH)	t_{ALEH}	400	–	– ns
Cycle time	T_{ALE}	–	2500	– ns
$\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ (Figs. 3 and 4)				
Control pulse width	t_{WL}	–	700	– ns
Address hold time	t_{LA}	80	–	– ns
Address set-up time	t_{AL}	120	–	– ns
Read cycle timings (Fig.3)				
ALE to read pulse delay time	t_{ALR}	80	–	– ns
Read pulse (falling edge) to data bus delay time	t_{RD}	–	–	500 ns
Data hold time	t_{DR}	0	–	200 ns
Write cycle timings (Fig.4)				
ALE to write pulse delay time	t_{ALW}	80	–	– ns
Address set-up time to $\overline{WR}$	t_{AW}	230	–	– ns
Data set up time before $\overline{WR}$	t_{DW}	500	–	– ns
Data hold time after $\overline{WR}$	t_{WD}	120	–	– ns

DEVELOPMENT SAMPLE DATA

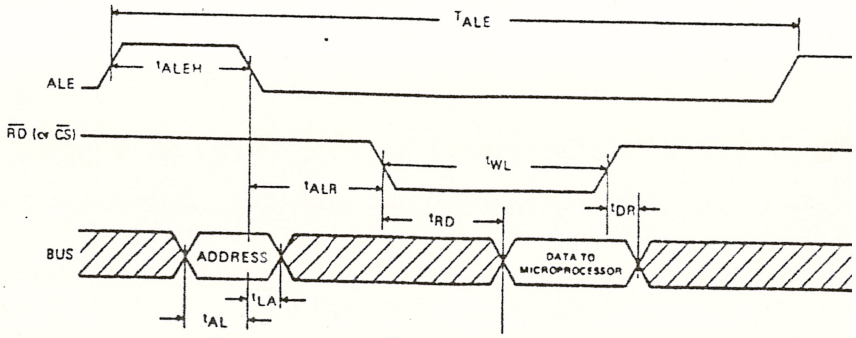

Fig.3 Read cycle timing

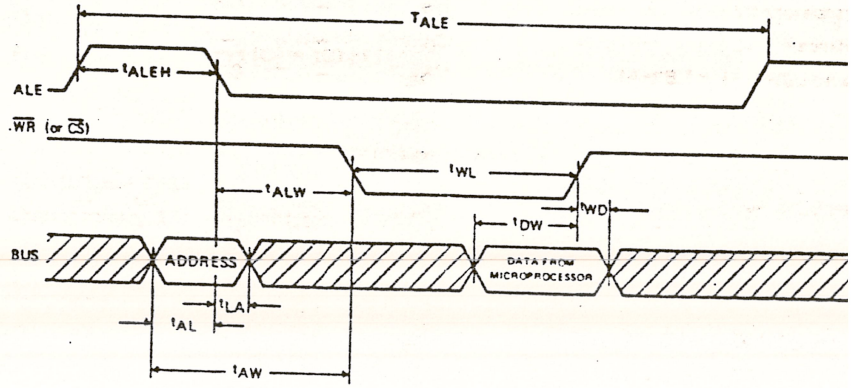

Fig.4 Write cycle timing

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

$\overline{DATA}$ B, DLIM B, $\overline{DLEN}$ B, IBCLCK (IBUS B)

			min.	typ.	max.	
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)	Fig.14	I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r | t_f	–	–	1	μs

other timings as IBUS A

DOCDI (open drain output)

Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)		I_{IR}	–	0.4	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	0.4	–	V

TXDATA

(Internal resistive pull-up, permitting wired - AND connection)

Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)		$-I_{IL}$	–	–	500	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)		V_{OH}	2.4	–	–	V
Load capacitance		C_L	–	–	40	pF
Output rise time (C_L = 40 pF)		t_r	–	3	–	μs

PA0 to PA4 (PORT A) (open drain output)

Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	13.2	V
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)		I_{OR}	–	–	10	μA
Load capacitance		C_L	–	–	40	pF
Fall time		t_f	–	–	1	μs

Inputs/Outputs (continued)

		min.	typ.	max.	
PB0 (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r | t_f	–	–	150	ns

Outputs

These are protected against connection to V_{SS} or V_{DD}.

FSKOUT and TFSKOUT

Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r | t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V

Autodialling timings are given in Fig.6

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.

An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 — I/O — 8-bit input/output port

Associated pins:

ALE	input	address latch enable from microprocessor
$\overline{WR}$	input	write pulse from microprocessor
$\overline{RD}$	input	read pulse from microprocessor
$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: — R8 — D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins:

DON	output	to drive dialling relays
IMP	output	to drive dialling relays

Operation

The autodial section includes a clock divider, a digit impulse counter, a sequence controller and an impulse generator (see block diagram Fig.5). A sequence to generate the impulses for one digit is initiated by setting D5 (DIAL GO) to '1', D3 to D0 to the binary code of the required digit, and D7 to the required mode. This initiates the sequence controller which loads the binary code into the digit impulse counter. The counter then generates the correct number of impulses at the rate of 10 per second, together with a DON pulse which overlaps the impulses by about 7 ms at the start and end (see Figs.6, 7); the interdigit pause period is also added by the sequence controller. D5 is reset to '0' at the end of a dialling sequence and may be read by the microprocessor to determine when the dial circuit is free to accept the next digit.

D7 (UK/$\overline{EUR}$) determines the mark/space ratio of the IMP pulses

UK = 2 off to 1 on
$\overline{EUR}$ = 1.5 off to 1 on
} both one pulse per 100 ms

There is a timer in the dial circuit which can be used to time out 1.5 seconds or 60 seconds by setting D4 or D6 respectively. These bits are read/write and are reset after the relevant time out period. In addition the 60 second timer can be reset by writing a '0' to D6. The 60 second timer may be used typically by the microprocessor to release the telephone line if connection has not been made within 60 seconds. The DON pulse resets the counter so that the time out is taken from the end of the last digit dialled. Once a dialling sequence for one digit has been initiated, R8 should be used only in read mode until D5 has been reset internally to '0' indicating the end of the dial sequence for that digit.

When D5 (DIAL GO) is set to '1' the carrier detect circuit (see the next section and Fig.8) is disabled.

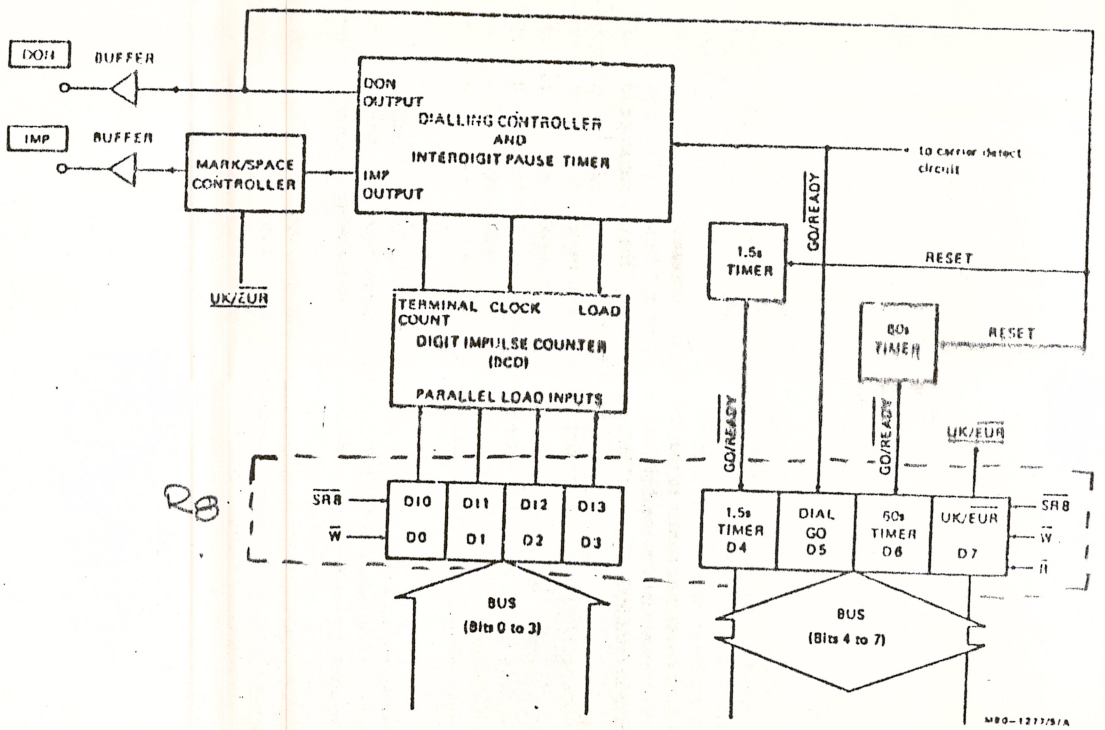

Fig.5 Autodial block diagram

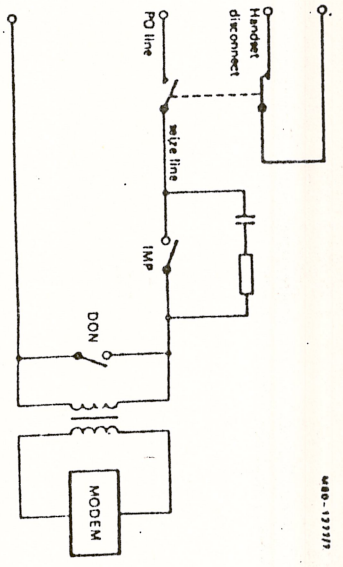

Fig.7 Simplified relay diagram

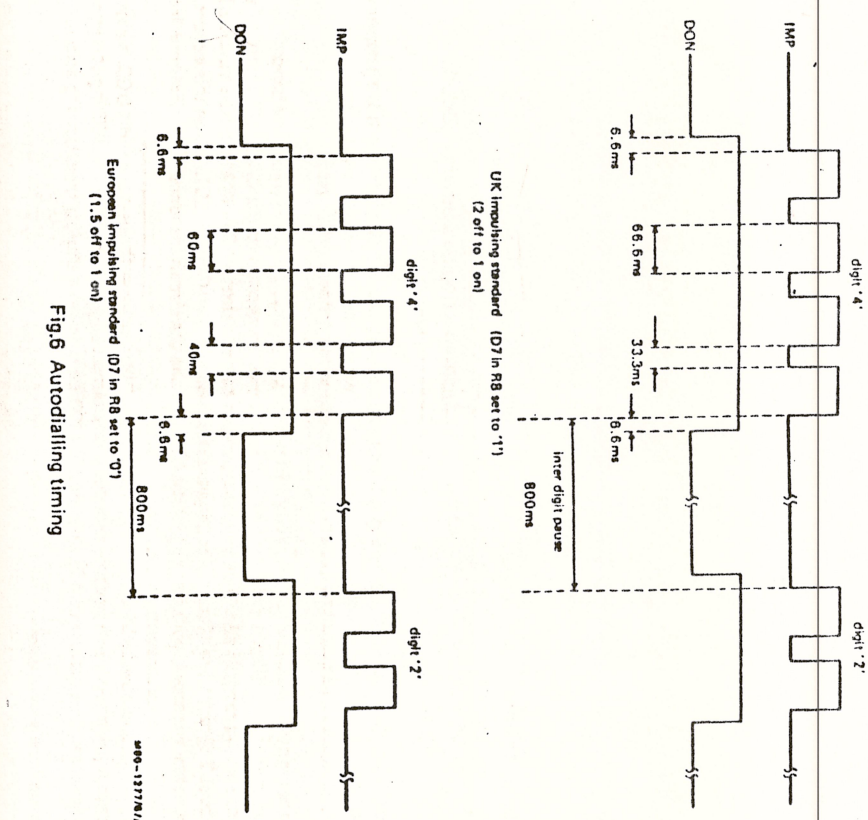

Fig.6 Autodialling timing

Line Demodulator and Carrier Detect (see Fig.8)

Associated Register:– None

Associated flags in other registers:

LIDCD	–	D2	–	R0 (Status)	–	instantaneous carrier detect flag
LDCD	–	D5	–	R0 (Status)	–	carrier detect flag
75/1200	–	D3	–	R2 (Mode)	–	transmit frequency baud rate (used in demodulator carrier detect circuit)
LDBEN	–	D4	–	R3 (Command)	–	line demodulator output buffer and carrier detect enable
DIAL GO	–	D5	–	R8 (Dial control)	–	used to disable carrier detect circuit during dialling sequence

Associated pins:

FSKIN	–	input	–	filtered, squared F.S.K. signal
CARDET	–	input	–	unfiltered (squared) F.S.K. signal.
DOCDI	–	input/output	–	demodulator output, external LDCD in

Operation

The input to the demodulator is the previously filtered and squared up F.S.K. signal from the telephone line. Its output is a pseudo analogue signal which must be externally filtered and squared to produce the demodulated data. The carrier detect circuit functions in the following modes:

a) Viewdata mode (1200 baud receive, 75 baud transmit). Initially, a narrow frequency band 'window' around 1300 Hz is accepted as carrier, this must be applied to the CARDET input. If a frequency in this range is present, the 'instantaneous carrier detected' flag will be HIGH (LIDCD), after about 2 seconds the 'line carrier detected' flag will be set HIGH (LDCD). When this occurs, the frequency window is widened to include 2100 Hz and the circuit no longer takes its input from the CARDET pin, but from the FSKIN pin.
If carrier is then removed LIDCD immediately goes LOW, and after about 1 second LDCD is reset, the frequency window again becomes narrow and around 1300 Hz and the CARDET input again becomes active. Reappearance of carrier in the 1300 Hz range will cause a repeat of the above.

b) 1200 baud each way mode
Only the instantaneous carrier detect is active in this mode. LDCD is forced LOW and the CARDET input inhibited (only FSKIN should be used in this mode).

c) External carrier detect input
If an external modem is used its (active LOW) carrier detect output is connected to DOCDI. Provided that the demodulator is not enabled, LDCD will be set if DOCDI is LOW and reset if it is HIGH.

Demodulator enable

LDCD is produced by the carrier detect circuit, which is enabled by LDBEN and disabled by DIAL GO. In the viewdata mode the demodulator is enabled by LDCD.
In the 1200 baud each way mode the demodulator is enabled directly by LDBEN.

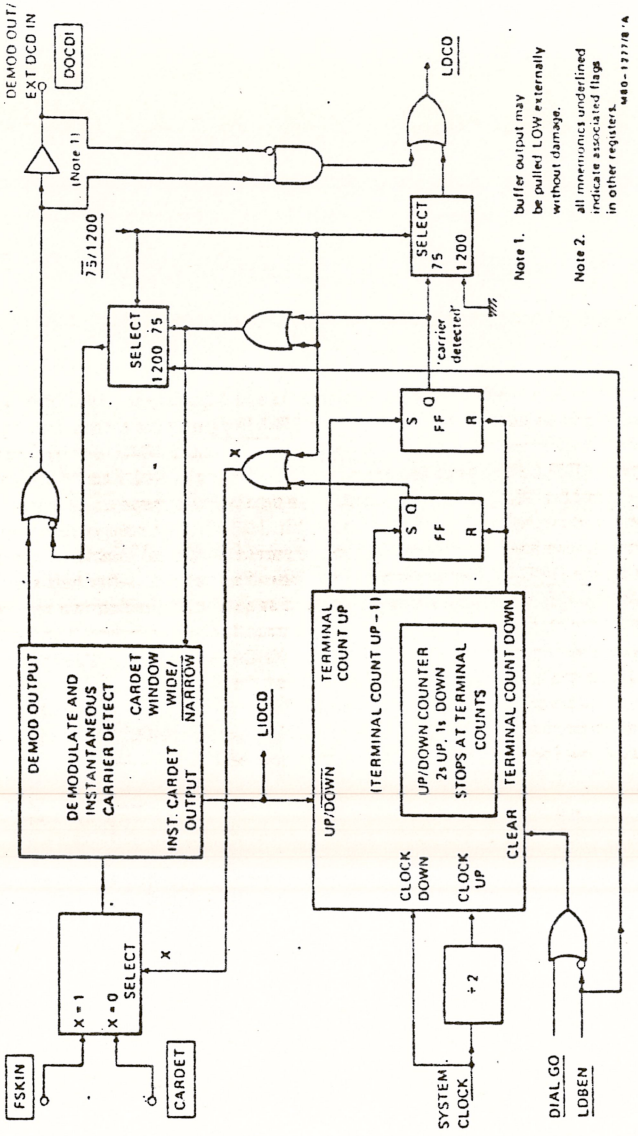

Fig.8 Line demodulator and carrier detect block diagram

Line Receiver (see Fig.9)

Associated Register: – R4 read only

Associated flags in other registers:

LRXRDY	–	D6	–	R0 (status)	–	valid data available in receive holding register
LFERR	–	D4	–	R0 (status)	–	line framing error (derived from STOP bit of message).
LPERR	–	D3	–	R0 (status)	–	line parity error.
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity detection mode select
$\overline{LPEN}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit plus parity mode select
LRXEN	–	D7	–	R3 (command)	–	line receiver enable.

Associated pins: RXDATA – input – received data input

Operation

The receiver may be configured to work with either 7 data bits and 1 parity, or with 8 data bits and no parity. Odd or even parity can be detected on chip, the LPERR flag being set when an error is detected. The required mode of operation should be selected by setting $\overline{LPEN}$ and LPO/$\overline{E}$ to the required states by writing to mode register (R2) before enabling the receiver by setting LRXEN to '1' in command register (R3). The data format is 10 bits per data word. The data word is made up of a start bit (LOW), 8 data bits, the 8th being an optional parity bit, and a stop bit (HIGH). The receive data will remain HIGH after the stop bit until the next data word. When the receiver has been enabled a negative transition is looked for on the RXDATA input indicating a possible start bit. After half a bit rate period the data is sampled again and if it is still LOW it is interpreted as a start bit, initiating a sequence which clocks the data into a shift register. When the full ten bit message has been received, the 8 data bits are parallel loaded into the receiver holding register (R4), the LRXRDY flag is set to '1'. The complement of the stop bit is loaded into the LFERR latch and the result of the parity check is loaded into LPERR latch. If line parity is not enabled i.e. $\overline{LPEN}$ = '1', then LPERR is held at '0'. The LRXRDY flag is reset to '0' after the microprocessor has read the receiver holding register (R4). The receiver has a 52 times baud rate factor to allow for maximum isochronous distortion.

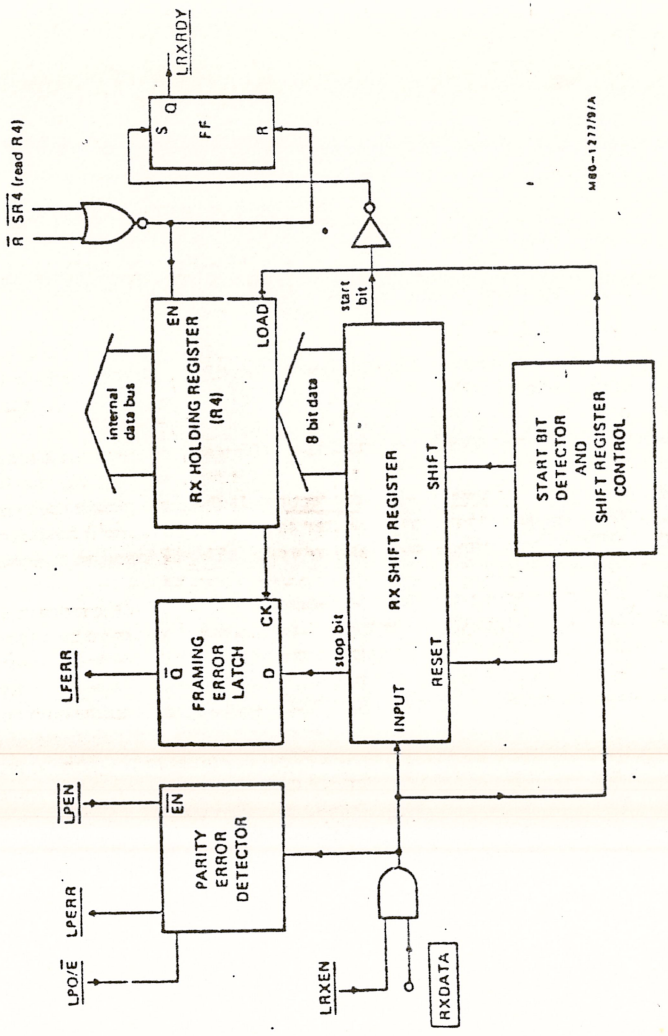

Fig.9 Line receiver block diagram

Line Transmitter (see Fig.10)

Associated Register: – R4 write only

Associated flags in other registers:

LTXRDY	–	D7	–	R0 (status)	–	transmit holding register ready to accept new data
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity mode select
$\overline{LPEN}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit data with parity mode select
$\overline{75}$/1200	–	D5	–	R2 (mode)	–	select transmit baud rate
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable

Associated pins: TXDATA – I/O – transmitter output (and also modulator input)

Operation

The data format of the transmitter is the same as that of the line receiver i.e. 10-bits, a start bit (LOW) followed by 8-data bits, the 8th bit being an optional parity (selected by LPEN), odd or even parity being selectable (by LPO/$\overline{E}$) ending with a STOP bit (HIGH) the output remaining HIGH until the next data word is written.

The transmitter and modulator may be used together or separately. The transmitter output is brought to the TXDATA pin (if LTXEN = 1) which is connected internally to the modulator input. The TXDATA pin has an internal resistive pull up permitting wire - AND connection. If the modulator is used with an off chip data source (e.g. UART) then data should not be written to the internal transmit holding register (R4). The STOP bit (HIGH) will then be continuously output when LTXEN = 1 (required to enable modulator output) allowing the external UART to control the TXDATA (pin 6).

To operate the transmitter the required mode should be set-up initially by writing to the mode register (R2) the required states of $\overline{75}$/1200, $\overline{LPEN}$, LPO/$\overline{E}$. The transmitter can then be enabled by setting LTXEN to '1' in the command register (R3). The 8-bit data word can then be written to the transmit holding register (R4). If parity is enabled then the 8th bit is ignored and the value of the parity bit calculated from the first 7-data bits and LPO/$\overline{E}$. The LTXRDY flag is set to zero when the holding register is written into. If the transmit output shift register is not currently in use the contents of the holding register are transferred to the output shift register and LTXRDY returns to '1'. This means that new data may now be written to the holding register but will not be transferred to the output shift register until the 10-bits of the current message have been clocked out. The start, stop, and parity bit (if selected) are written into the output shift register with the data word automatically.

Two transmit baud rates are selectable, 75 baud for viewdata transmissions or 1200 baud for private data communication systems.

DEVELOPMENT SAMPLE DATA

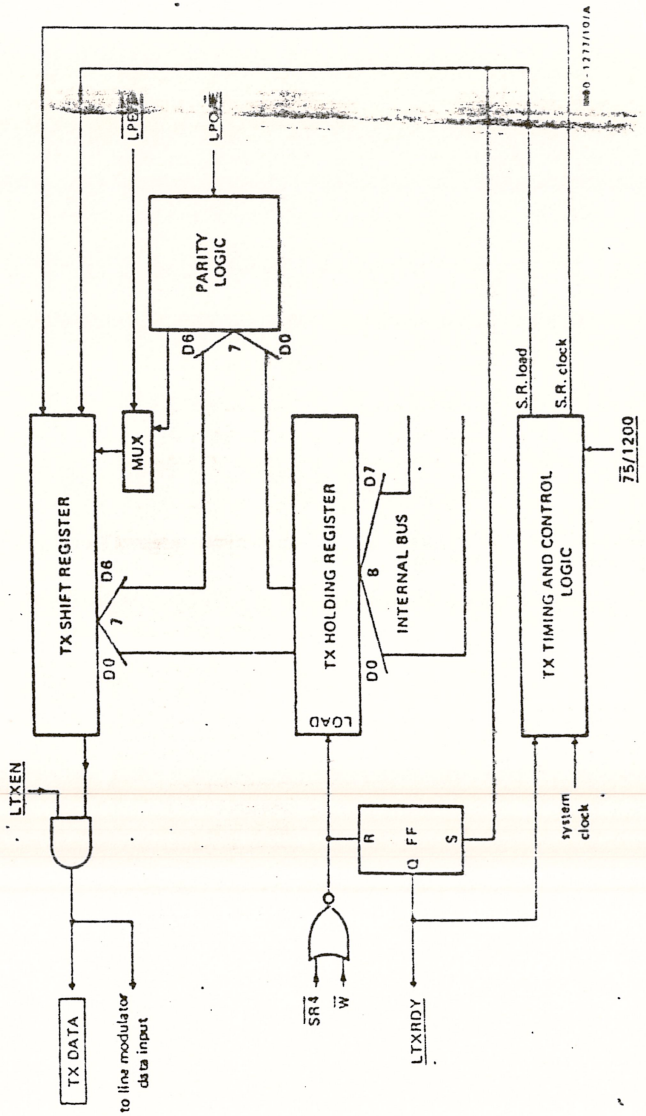

Fig.10 Line transmitter block diagram